PATENT ABSTRACTS OF JAPAN

(11)Publication number : 08-160387
(43)Date of publication of application : 21.06.1996

(51)Int.Cl. G02F 1/133
G02F 1/133
G09G 3/36
H01L 29/786
H01L 21/336

(21)Application number : 07-219558
(22)Date of filing : 04.08.1995

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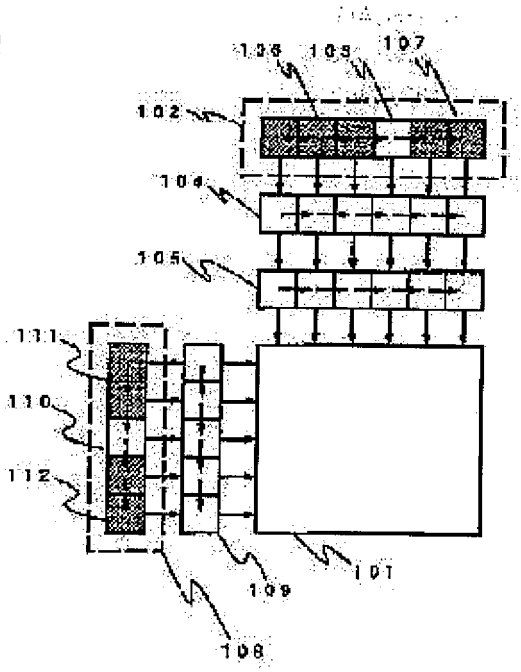
(30)Priority
Priority number : 06214258 Priority date : 16.08.1994 Priority country : JP
06270564 07.10.1994 JP

(54) PERIPHERAL DRIVING CIRCUIT OF LIQUID CRYSTAL ELECTROOPTICAL DEVICE

(57)Abstract:
PURPOSE: To reduce power consumption of a peripheral driving circuit.
CONSTITUTION: A liquid crystal display section 101, a signal line driving circuit and a peripheral driving circuit are provided on the same substrate. When a signal is inputted to a register 103 of the Nth stage of a shift register 102 of the signal line driving circuit, power supply is stopped to a register 106 preceding to the (N-1)th stage in which transmission of a signal is finished and a register 107 succeeding to the (N+1)th stage in which input of a signal is stood by. On the other hand, when a signal is inputted to a register 110 of the Nth stage of a shift register 108 of a scanning line driving circuit, power supply to a register 111 preceding to the (N-1)th stage is stopped and a register 112 of the (N+1) th post stage.



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CLAIMS

[Claim(s)]

[Claim 1]A circumference drive circuit of a liquid crystal electro-optic device when a signal is inputted into one of said the registers in a circumference drive circuit of a liquid crystal electro-optic device characterized by comprising the following, wherein said power supplying circuit stops an electric power supply to at least one register other than the register concerned.
A shift register circuit constituted by connecting two or more steps of registers.
A power supplying circuit which supplies electric power to said register.

[Claim 2]A circumference drive circuit of a liquid crystal electro-optic device, wherein said shift register circuit is constituted by a P channel type thin film transistor and resistance in claim 1.
[Claim 3]A circumference drive circuit of a liquid crystal electro-optic device, wherein said power supplying circuit controls an electric power supply to said register in claim 1 according to an output of said shift register circuit.
[Claim 4]A circumference drive circuit of a liquid crystal electro-optic device, wherein said power supplying circuit is constituted by a P channel type thin film transistor, resistance, and a capacitor in claim 1.
[Claim 5]A circumference drive circuit of a liquid crystal electro-optic device characterized by power consumption of said power supplying circuit being below power consumption of said shift-register-circuit way in claim 1.
[Claim 6]In a circumference drive circuit of a liquid crystal electro-optic device characterized by comprising the following, it is the Nth step.
A shift register circuit constituted by connecting two or more steps of registers.
A power supplying circuit which supplies electric power to said register.
A circumference drive circuit of a liquid crystal electro-optic device when, as for [N, a signal is inputted into a register of natural number], wherein said power supplying circuit stops an electric power supply to at least one register of registers other than the Nth step.
[Claim 7]A circumference drive circuit of a liquid crystal electro-optic device, wherein said shift register circuit is constituted by a P channel type thin film transistor and resistance in claim 6.
[Claim 8]A circumference drive circuit of a liquid crystal electro-optic device, wherein said power supplying circuit controls an electric power supply to said register in claim 6 according to an output of said shift register circuit.
[Claim 9]A circumference drive circuit of a liquid crystal electro-optic device, wherein said power supplying circuit is constituted by a P channel type thin film transistor, resistance, and a capacitor in claim 6.
[Claim 10]A circumference drive circuit of a liquid crystal electro-optic device characterized by power consumption of said power supplying circuit being below power consumption of said shift-register-circuit way in claim 6.
[Claim 11]In a circumference drive circuit of a liquid crystal electro-optic device characterized by comprising the following, it is the Nth step.
A shift register circuit constituted by connecting two or more steps of registers.
A power supplying circuit which supplies electric power to said register.
A circumference drive circuit of a liquid crystal electro-optic device when, as for [N, a signal is inputted into a register of natural number], wherein said power supplying circuit stops an electric power supply to a register before a ** (N-2) stage, and a register after a ** (N+2) stage.
[Claim 12]A circumference drive circuit of a liquid crystal electro-optic device, wherein said shift register circuit comprises a P channel type thin film transistor and resistance in claim 11.
[Claim 13]A circumference drive circuit of a liquid crystal electro-optic device, wherein said power supplying circuit controls an electric power supply to said register in claim 11 according to an output of said shift register circuit.
[Claim 14]A circumference drive circuit of a liquid crystal electro-optic device, wherein said power supplying circuit is constituted by a P channel type thin film transistor, resistance, and a capacitor in claim 11.
[Claim 15]A circumference drive circuit of a liquid crystal electro-optic device characterized by power consumption of said power supplying circuit being below power consumption of said shift-

register-circuit way in claim 11.
[Claim 16]In a circumference drive circuit of a liquid crystal electro-optic device characterized by comprising the following, it is the Nth step.
A shift register circuit constituted by connecting two or more steps of registers.
A power supplying circuit which supplies electric power to said register.
When a signal is inputted into a register of natural number] as for [N, said power supplying circuit is a ** (N-x) stage. [x>=2] A former register and a ** (N+y) stage [y>=2] A circumference drive circuit of a liquid crystal electro-optic device stopping an electric power supply to subsequent registers.
[Claim 17]A circumference drive circuit of a liquid crystal electro-optic device, wherein said shift register circuit is constituted by a P channel type thin film transistor and resistance in claim 16.
[Claim 18]A circumference drive circuit of a liquid crystal electro-optic device, wherein said power supplying circuit controls an electric power supply to said register in claim 16 according to an output of said shift register circuit.
[Claim 19]A circumference drive circuit of a liquid crystal electro-optic device, wherein said power supplying circuit is constituted by a P channel type thin film transistor, resistance, and a capacitor in claim 16.
[Claim 20]A circumference drive circuit of a liquid crystal electro-optic device characterized by power consumption of said power supplying circuit being below power consumption of said shift register circuit in claim 16.
[Claim 21]A block which two or more steps of registers were connected, and was constituted.
A shift register circuit which this block was connected two or more steps, and was constituted.
A power supplying circuit which is connected for said every block and supplies electric power to said register.
When a signal is inputted into a register which is a circumference drive circuit of a liquid crystal electro-optic device provided with the above, and constitutes one of said the blocks, said power supply circuit stops electric power supplies other than the block concerned.

[Claim 22]A circumference drive circuit of a liquid crystal electro-optic device, wherein said shift register circuit is constituted by a P channel type thin film transistor and resistance in claim 21.
[Claim 23]A circumference drive circuit of a liquid crystal electro-optic device characterized by power consumption of said power supplying circuit being below power consumption of said shift register circuit in claim 21.
[Claim 24]In a circumference drive circuit of a liquid crystal electro-optic device which specifies a pixel of a picture element part, have an electric power supply drive circuit which supplies electric power to this circumference drive circuit, and said power supplying circuit, A circumference drive circuit of a liquid crystal electro-optic device stopping electric power supplies other than a circumference drive circuit which specifies said pixel through which it passes in part at least.
[Claim 25]A circumference drive circuit of a liquid crystal electro-optic device, wherein said circumference drive circuit is constituted by a thin film transistor of one conductivity type, resistance, and a capacitor in claim 24.
[Claim 26]A circumference drive circuit of a liquid crystal electro-optic device, wherein said power supplying circuit is constituted by a thin film transistor of one conductivity type, resistance, and a capacitor in claim 24.
[Claim 27]In a circumference drive circuit of a liquid crystal electro-optic device which specifies a pixel of a picture element part, have an electric power supply drive circuit which supplies electric power to this circumference drive circuit, and this power supplying circuit, A circumference drive circuit of a liquid crystal electro-optic device dropping service voltage other than a circumference drive circuit which specifies said pixel through which it passes in part at least.
[Claim 28]A circumference drive circuit of a liquid crystal electro-optic device, wherein a circumference drive circuit has a thin film transistor of one conductivity type, and the shift register which comprised resistance in claim 27.
[Claim 29]A circumference drive circuit of a liquid crystal electro-optic device, wherein said

power supplying circuit is constituted by a thin film transistor of one conductivity type, resistance, and a capacitor in claim 27.
[Claim 30]In a circumference drive circuit which drives a picture element part of a liquid crystal optical device, it has any at least one of a scanning line driving circuit or the signal line driving circuits, and an electric power supply drive circuit which supplies electric power to said circumference drive circuit, and said scanning line driving circuit is the Nth of said picture element part about voltage. When impressed by a pixel of natural number], [N, Or when sampling a video signal and outputting to the Nth pixel of said picture element part by said signal line driving circuit, said power supplying circuit, A circumference drive circuit of a liquid crystal electro-optic device falling electric power supplied to a portion corresponding to a pixel of ** (N+1) watch henceforth, and a portion corresponding to a pixel of ** (N-2) watch before to said circumference drive circuit.
[Claim 31]A circumference drive circuit of a liquid crystal electro-optic device, wherein a circumference drive circuit has a thin film transistor of one conductivity type, and the shift register which comprised resistance in claim 30.
[Claim 32]A circumference drive circuit of a liquid crystal electro-optic device, wherein said power supplying circuit is constituted by a thin film transistor of one conductivity type, resistance, and a capacitor in claim 30.
[Claim 33]In a circumference drive circuit which drives a picture element part of a liquid crystal optical device, it has an electric power supply drive circuit which supplies electric power to said circumference drive circuit, and is the Nth of said picture element part. When voltage is impressed to a pixel of natural number], [N, Or when a video signal sampled by the Nth pixel of said picture element part is written in, said power supplying circuit, A circumference drive circuit of a liquid crystal electro-optic device falling electric power supplied to a portion corresponding to a pixel of eye ** (N+x) watch of ** [x>=1], and a portion corresponding to a pixel of eye ** (N-y) watch [y>=2] to said circumference drive circuit.
[Claim 34]A circumference drive circuit of a liquid crystal electro-optic device, wherein said circumference drive circuit is constituted by a thin film transistor of one conductivity type, and resistance in claim 33.
[Claim 35]A circumference drive circuit of a liquid crystal electro-optic device, wherein said power supplying circuit is constituted by a thin film transistor of one conductivity type, resistance, and a capacitor in claim 33.
[Claim 36]In a circumference drive circuit of a liquid crystal electro-optic device for driving a picture element part divided into two or more blocks so that two or more pixels might be arranged on a matrix and might contain said at least one pixel, Have a power supplying circuit which supplies electric power to this circumference drive circuit, and during said block, When a pixel in which voltage is impressed or a sampled BIO signal is written does not exist, Or a circumference drive circuit of a liquid crystal electro-optic device characterized by a thing to which said power supplying circuit corresponds to a pixel under said block among said circumference drive circuits when a pixel in which a sampled video signal is written does not exist, and which it receives in part at least and is suspended for an electric power supply.
[Claim 37]Claim 36 comprising:
Said circumference drive circuit is a thin film transistor of one conductivity type.
A counter and a decoder which are constituted by resistance.

[Claim 38]A circumference drive circuit of a liquid crystal electro-optic device, wherein said power supplying circuit is constituted by a thin film transistor of one conductivity type, resistance, and a capacitor in claim 36.
[Claim 39]Two or more pixels are arranged at matrix form, in a circumference drive circuit of a liquid crystal electro-optic device for driving a picture element part divided into two or more blocks, it has a power supplying circuit which supplies electric power to this circumference drive circuit so that said at least one pixel may be included, and it is the Nth. When a pixel in which a video signal sampled when a pixel by which voltage is impressed during a block of natural number] existed is written exists, [N said power supplying circuit, A circumference drive circuit of a liquid crystal electro-optic device stopping an electric power supply to a circumference

drive circuit corresponding to a pixel contained in at least one block of a block of ** (N+1) watch henceforth, and (N-1) said block of watch before.
[Claim 40]Claim 39 comprising:
Said circumference drive circuit is a thin film transistor of one conductivity type.
A counter and a decoder which were constituted by resistance.

[Claim 41]A circumference drive circuit of a liquid crystal electro-optic device, wherein said power supplying circuit is constituted by a thin film transistor of one conductivity type, resistance, and a capacitor in claim 39.
[Claim 42]Two or more pixels are arranged at matrix form, in a circumference drive circuit of a liquid crystal electro-optic device for driving a picture element part divided into two or more blocks, it has a power supplying circuit which supplies electric power to this circumference drive circuit so that said at least one pixel may be included, and it is the Nth. When a pixel to which voltage is impressed exists by said circumference drive circuit during a block of natural number], [N by said circumference drive circuit. When a pixel in which a sampled video signal is written exists, said power supplying circuit, A circumference drive circuit of a liquid crystal electro-optic device stopping an electric power supply to a circumference drive circuit corresponding to a pixel contained in at least one block of a block of henceforth ** (N+x) watch [x>=1], and a block of before ** (N-y) watch [y>=1].
[Claim 43]Claim 42 comprising:
Said circumference drive circuit is a thin film transistor of one conductivity type.
A counter and a decoder which were constituted by resistance.

[Claim 44]A circumference drive circuit of a liquid crystal electro-optic device, wherein said power supplying circuit is constituted by a thin film transistor of one conductivity type, resistance, and a capacitor in claim 42.
[Claim 45]In a circumference drive circuit of a liquid crystal electro-optic device for driving a picture element part divided into two or more blocks so that two or more pixels might be arranged on a matrix and might contain said at least one pixel, Have a power supplying circuit which supplies electric power to this circumference drive circuit, and during said block, When a pixel in which voltage is impressed or a sampled video signal is written does not exist, Or a circumference drive circuit of a liquid crystal electro-optic device characterized by said power supplying circuit lowering at least electric power corresponding to a pixel under said block which receives in part and is supplied among said circumference drive circuits when a pixel in which a sampled video signal is written does not exist.
[Claim 46]Claim 45 comprising:
Said circumference drive circuit is a thin film transistor of one conductivity type.
A counter and a decoder which are constituted by resistance.

[Claim 47]A circumference drive circuit of a liquid crystal electro-optic device, wherein said power supplying circuit is constituted by a thin film transistor of one conductivity type, resistance, and a capacitor in claim 45.
[Claim 48]Two or more pixels are arranged at matrix form, in a circumference drive circuit of a liquid crystal electro-optic device for driving a picture element part divided into two or more blocks, it has a power supplying circuit which supplies electric power to this circumference drive circuit so that said at least one pixel may be included, and it is the Nth. When a pixel to which voltage is impressed exists by said circumference drive circuit during a block of natural number], [N by or said circumference drive circuit. When a pixel in which a sampled video signal is written exists, said power supplying circuit, A circumference drive circuit of a liquid crystal electro-optic device lowering power supply to a circumference drive circuit corresponding to a pixel contained in at least one block of a block of ** (N+1) watch henceforth, and (N-1) said block of watch before.
[Claim 49]Claim 48 comprising:
Said circumference drive circuit is a thin film transistor of one conductivity type.
A counter and a decoder which were constituted by resistance.

[Claim 50]A circumference drive circuit of a liquid crystal electro-optic device, wherein said power supplying circuit is constituted by a thin film transistor of one conductivity type, resistance, and a capacitor in claim 48.
[Claim 51]Two or more pixels are arranged at matrix form, in a circumference drive circuit of a liquid crystal electro-optic device for driving a picture element part divided into two or more blocks, it has a power supplying circuit which supplies electric power to said circumference drive circuit so that said at least one pixel may be included, and it is the Nth. When a pixel to which voltage is impressed exists by said circumference drive circuit during a block of natural number], [N by said circumference drive circuit. When a pixel in which a sampled video signal is written exists, said power supplying circuit, A circumference drive circuit of a liquid crystal electro-optic device lowering ********** to a circumference drive circuit corresponding to a pixel contained in at least one block of a block of henceforth ** (N+x) watch [x>=1], and a block of before ** (N-y) watch [y>=1].
[Claim 52]Claim 51 comprising:
Said circumference drive circuit is a thin film transistor of one conductivity type.
A counter and a decoder which were constituted by resistance.

[Claim 53]A circumference drive circuit of a liquid crystal electro-optic device, wherein said power supplying circuit is constituted by a thin film transistor of one conductivity type, resistance, and a capacitor in claim 51.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application]The invention indicated on these specifications relates to the circumference drive for driving the picture element part of a liquid crystal electro-optic device. It is related with the circumference drive circuit of the liquid crystal electro-optic device which should operate with low power consumption especially.
[0002]
[Conventional example] Drawing 29 is an outline lineblock diagram of the liquid crystal electro-optic device generally known, and a liquid crystal electro-optic device, It is constituted by the signal line driving circuit (2902) and scanning line driving circuit (2903) for driving the picture-element-matrix part (2901) which displays a picture, and a picture-element-matrix part (2901). The picture element matrix (2901) is connected to the scanning line driving circuit (2903) and the signal line driving circuit (2902) by the scanning line (2904) and the signal wire (2905), respectively.
[0003]In the picture-element-matrix part (2901), the scanning line (2904) and the signal wire (2905) are arranged at matrix form. In particular, in the active-matrix type liquid crystal display, the pixel thin film transistor (a thin film transistor is hereafter abbreviated to TFT) (2906) is arranged at the crossing portion. The gate electrode of the pixel TFT (2906) is connected to a

scanning line (2904), a source electrode is connected to a signal wire (2905), and the drain electrode is connected to the picture element electrode of liquid crystal capacity (2907). Retention volume (2908) is connected to liquid crystal capacity (2907) in parallel. Since there is no liquid crystal capacity (2907) of Rie in a big electric capacity value, an electric charge is held in retention volume (2908).

[0004]The signal line driving circuit (2902) comprises a shift register circuit (2909), a buffer circuit (2910), and a sampling circuit (2911). On the other hand, the scanning line driving circuit (2903) is constituted by the shift register (2916) and the NAND circuit inverter type buffer (2917).

[0005]Drawing 30 (a) and drawing 30 (b) are a shift register circuit (2909) and a circuit diagram of (2916), Drawing 30 (a) is a circuit diagram of the shift register circuit constituted with the clocked inverter (3001), and drawing 30 (b) is a circuit diagram of the shift register circuit constituted by the transmission gate (3002).

[0006]When displaying a picture on a picture-element-matrix part (2901), in a signal line driving circuit (2902), the signal in sync with a video signal is inputted into a shift register (2909) from an input terminal (2912). With the register of a shift register (2909), this input signal is shifted one by one according to a clock pulse, and is inputted and memorized in the buffer circuit (2910) of inverter form. As for the analog switch (2913) of a sampling circuit (2911), one and OFF are controlled by a buffer circuit (2910).

[0007]If a video signal line (2915) and retention volume (2914) will connect too hastily, and an electric charge will be charged by retention volume (2914), if an analog switch (2913) is turned on, and turned off, an electric charge will be held as a video signal sampled by retention volume (2914). Again, if an analog switch (2913) is turned on, the electric charge of retention volume (2914) will discharge and the video signal sampled by the pixel TFT (2906) will be transmitted via a signal wire (2905).

[0008]According to the clock which synchronized with the input signal in sync with a Vertical Synchronizing signal, and the Horizontal Synchronizing signal in the scanning line driving circuit (2903), with a shift register (2916) and a NAND circuit inverter type buffer (2917). A scanning line (2904) is driven one by one, and turning on and off of the pixel TFT (2906) is controlled.

[0009]With a scanning line (2904), if the voltage exceeding threshold voltage is impressed to the gate electrode of the pixel TFT (2906), the pixel TFT (2906) will be in an ON state, and the drain electrode and source electrode of the pixel TFT (2906) will be in a short condition. In this state, the video signal sampled by the pixel TFT (2906) via the signal wire (2905) from retention volume (2914) is transmitted, and liquid crystal capacity (2907) and retention volume (2908) are charged. If the pixel TFT (2906) will be in an OFF state, the drain electrode of the pixel TFT (2906) will be in an opened condition, and the electric charge accumulated in liquid crystal capacity (2907) and retention volume (2908) will be held until the pixel TFT (2906) is turned on next.

[0010]In a signal line driving circuit (2903) and a scanning line driving circuit (2902), a decoder circuit can also be used instead of a shift register circuit (2909) and (2916).

[0011]Drawing 31 is a circuit diagram of the signal line driving circuit constituted using the decoder circuit. In this case, a pixel and an address are made to correspond to 1 to 1. When writing a video signal in a pixel, address signal ** is inputted via an address signal entrance cable (3101) in a signal line driving circuit. According to an address signal, a NAND gate (3102) chooses a signal wire and outputs a signal to an analog switch (3103). In an analog switch (3103), cause **** of the turning on and off of retention volume (3104) is carried out, a video signal is sampled, and it is held as an electric charge at retention volume (3104).

[0012]Or in a signal line driving circuit (2903) and a scanning line driving circuit (2902), a decoder circuit and a counter circuit can also be used instead of a shift register circuit (2909) and (2916).

[0013]Drawing 32 is a circuit diagram of the signal line driving circuit constituted by the decoder circuit and the counter circuit. A counter circuit (3202) calculates a clock pulse input (3201), and inputs it into a NAND gate (3203) by making this ********** into an address signal. According to an address signal, a NAND gate (3203) chooses a signal wire and inputs a signal into a corresponding analog switch (3204). In an analog switch (3204), if the signal from a NAND gate (3203) is inputted, a video signal will be sampled and it will hold as an electric charge to retention

volume (3205).
[0014]Conventionally, the circumference drive circuit of a liquid crystal electro-optic device is produced in the CMOS circuit on the transparent substrate in which the picture element matrix was formed. Drawing 33 is a circuitry figure of the shift register constituted by the CMOS circuit, and corresponds to the shift register shown in drawing 30 (a).
[0015]When a CMOS circuit constitutes a peripheral circuit, in order to manufacture P channel type TFT and N channel type TFT to the same substrate, the problem that a process increases arises. There is a fault on the characteristic that the characteristic does not gather easily due to P channel type TFT and N channel type TFT.
[0016]In the former, in order to solve the above-mentioned problem, elements, such as TFT of one conductivity type and resistance, constitute a circumference drive circuit, and simplification of a process and equalization of the characteristic of an element are attained.
[0017]Drawing 34 is a lineblock diagram of the shift register circuit constituted by P channel type TFT and resistance. Drawing 35 is a lineblock diagram of the basic gate circuit which used P channel type TFT and resistance, and shows the lineblock diagram of a NAND circuit, a NOR circuit, and an inverter circuit. These basic circuits can constitute JK-flip-flop, a counter circuit, etc. Drawing 36 is a lineblock diagram of JK-flip-flop, and drawing 37 is a lineblock diagram of 4 bit counter circuits.
[0018]Four bit counter circuits shown in drawing 37 create bit output Q_1 of the output signal of a ripple carry, and a counter - Q_4, and its inverted output signal according to a power supply, a clearance, a clock, and the input signal of each enabling, respectively.
[0019]
[Problem(s) to be Solved by the Invention]However, there is a problem that the circumference drive circuit using P channel type TFT and resistance has large power consumption. For example, if P channel type TFT (3401) is turned on, a ground (3403) will connect with a power supply (3402) too hastily by resistance (3404), penetration current will flow, and, as for the shift register circuit shown in drawing 34, power consumption will become large.
[0020]If the resistance of resistance (3404) is enlarged and it is made not to send current, it will become difficult to discharge, it will become late to change from power supply potential to ground potential, and a frequency characteristic will worsen. In the former, in order to give priority to a frequency characteristic, it is difficult to make resistance (3404) into a big value.
[0021]It becomes a serious obstacle that power consumption is large, when using for electronic equipment, such as a portable information device.
[0022]Even if the purpose of this invention uses the big circumference drive circuit of power consumption, there is in providing the circumference drive circuit of the liquid crystal electro-optic device which can reduce the power consumption needed when driving the whole liquid crystal electro-optic device.
[0023]
[Means for Solving the Problem and its Function]In order to solve an above-mentioned problem, composition of a circumference drive circuit of a liquid crystal electro-optic device concerning this invention, In a circumference drive circuit of a liquid crystal electro-optic device which has a shift register circuit constituted by connecting two or more steps of registers, and a power supplying circuit which supplies electric power to said register, When a signal is inputted into one of said the registers, said power supplying circuit stops an electric power supply to at least one register other than the register concerned.
[0024]Synchronizing with a clock signal, a shift register of a circumference drive circuit of a liquid crystal electro-optic device is delayed by a register, and is transmitting one signal one by one. Therefore, it is functioning [whole / a part of] as a shift register. Therefore, this invention supplies electric power only to a register which is functioning, and he is trying to reduce power consumption of the whole circumference drive circuit.
[0025]An operation of a circumference drive circuit which has the above-mentioned composition is explained based on drawing 1. Drawing 1 is a lineblock diagram of a liquid crystal display, and a liquid crystal display section (101), a signal line driving circuit, and a circumference drive circuit are provided in the shape of same board. In a signal line driving circuit, a shift register (102), a buffer (104), and a sampler (105) which comprise two or more steps of registers are connected

one by one, and an output of a sampler (105) is connected to a liquid crystal display section (101) via a signal wire. On the other hand, in a scanning line driving circuit, a shift register (108) and a buffer (109) are connected one by one, and an output of a buffer (109) is connected to a liquid crystal display section (101) via a scanning line.

[0026]In a signal line driving circuit, when a signal is inputted into a register (103) of the Nth step of a shift register (102), It is possible to stop an electric power supply to a register (106) before a final stage of a buffer (104) and a ** (N-1) stage after ending transfer of a signal, maintaining electric power so that there may be no influence in a sampler (105).

[0027]It is also possible to stop an electric power supply to a register (107) of the ** (N+1) stage henceforth are standing by an input of a signal.

[0028]When a register (110) of the Nth step has an input signal, maintaining electric power so that there may be no influence in a buffer (109) similarly about a shift register (108) of a scanning line driving circuit, It is possible to stop an electric power supply to a register (111) of ** (N-1) stage before and a register (112) of ** (N+1) stage henceforth.

[0029]When it constitutes so that an output of two steps of adjacent registers may become active simultaneously in a shift register of a circumference drive circuit, When an input signal reaches a register of the Nth step, since an output of a register of a ** (N-1) stage is also active, an electric power supply to a register before a ** (N-2) stage can be stopped.

[0030]In ensuring pulse width by one cycle of a clock, When a signal inputs into a register of the Nth step, it is begun to supply a power supply to a register of eye a ** (N+1) stage are not outputting an active signal, and carries out based on the next clock change as [transmit / a signal / to a register of eye a ** (N+1) stage / certainly]. Therefore, when a signal is inputted into a register of the Nth step, it is possible to stop an electric power supply to a register after a ** (N+2) stage. in addition -- a case where changing pulse width of an input signal is allowed by element delay -- an electric power supply to a register of ** (N+1) stage henceforth -- a stop -- things become possible.

[0031]When it gives priority to decreasing an element number rather than reducing power consumption, when an input signal reaches a register of the Nth step, it is not necessarily necessary to restrict a register which stops an electric power supply to a register of ** (N+2) stage henceforth before [** (N-2) stage].

[0032]For example, it is also possible to continue an electric power supply to a register of eye a ** (N-2) stage, and not to make an electric power supply registers, such as eye a ** (N-3) stage and eye a ** (N-4) stage. Therefore, ** (N-x) stage It is possible even if it stops an electric power supply to a shift register of [x>=2].

[0033]When an input signal reaches a register of the Nth step, it is also possible to supply a power supply to a register of eye a ** (N+2) stage, and not to supply electric power to registers, such as a ** (N+3) stage and a ** (N+4) stage. Therefore, eye a ** (N+y) stage It is possible even if it stops an electric power supply to a register of [y>=2].

[0034]For example, since only a portion which should function is operated although each circuit has large power consumption when a P channel type thin film transistor and resistance constitute a shift register circuit and a power supplying circuit, power consumption can be stopped as a whole. As for especially power consumption of a power supplying circuit which is always operating, it is preferred to make it smaller than power consumption of a shift register circuit.

[0035]Other composition of a circumference drive circuit of a liquid crystal electro-optic device concerning this invention, A block which two or more steps of registers were connected, and was constituted, and a shift register circuit which this block was connected two or more steps, and was constituted, In a circumference drive circuit of a liquid crystal electro-optic device which has a power supplying circuit which is connected for said every block and supplies electric power to said register, When a signal is inputted into a register which constitutes one of said the blocks, said power supply circuit stops electric power supplies other than the block concerned.

[0036]In a shift register, a circumference drive circuit which has the above-mentioned composition packs arbitrary numbers of registers, blocks **, and controls an electric power supply for every block. By adopting this composition, a control circuit can be made simple rather than controlling one step of register at a time.

[0037]An operation of a circumference drive circuit which has the above-mentioned composition is explained based on drawing 2. Some steps of registers of a shift register (201) are packed, and register block (202) - (204) is formed. A control circuit (205) supplies control signal (206) - (208) for every register block.
[0038]A control signal (208) which supplies electric power is inputted into a shift register block (204) in which a register into which an input signal (209) which should be shifted is inputted exists, and electric power is supplied to it. A signal (206) which stops an electric power supply, and (207) are inputted into a register block (202) after transmitting an input signal which should be shifted, and a register block (203) which is standing by an input of a signal, and an electric power supply is stopped.
[0039]Although the period when the above-mentioned composition is delivering an input signal during two blocks must supply electric power to these blocks, electric power may be supplied to one block with an input signal, and an electric power supply to a block without an input signal may stop.
[0040]Other composition of a circumference drive circuit of a liquid crystal electro-optic device concerning this invention, In a circumference drive circuit of a liquid crystal electro-optic device which specifies a pixel of a picture element part, have an electric power supply drive circuit which supplies electric power to this circumference drive circuit, and said power supplying circuit, Stopping electric power supplies other than a circumference drive circuit which specifies said pixel through which it passes in part at least, or power supply is lowered.
[0041]A portion as which a circumference drive circuit of a liquid crystal electro-optic device which has the above-mentioned composition does not specify a portion on which a circumference drive circuit is not functioning, i.e., a pixel, stops an electric power supply, or he is trying to lower power supply.
[0042]In this specification, it says specifying a pixel sampling a video signal in a signal line driving circuit, and charging retention volume. Or in a scanning line driving circuit, it says making into an ON state the pixel TFT connected to a scanning line.
[0043]Numerals are attached for a circuit which specifies a pixel first one by one as 1st circuit. If an input signal arrives at the Nth circuit, while outputting of the Nth circuit will become active, a circuit of eye ** (N-1) watch also serves as an active output. Therefore, in circuits other than these, since it is not an active output, power supply can be lowered. That is, an electric power supply to a circuit part of ** (N-2) watch before is stopped, or power supply can be lowered. An electric power supply to a circuit part of ** (N+1) watch henceforth is stopped, or power supply can be lowered.
[0044]An electric power supply to a circuit of eye ** (N+1) watch remains as it is, stops an electric power supply to circuit parts, such as eye ** (N+2) watch and eye ** (N+3) watch, or can lower power supply. Therefore, ** (N+x) stage It is also possible to stop an electric power supply to a circuit of [x>=1], or to lower power supply.
[0045]Or it supplies a power supply to a circuit of eye a ** (N-2) stage and does not supply electric power to circuits, such as a ** (N-2) stage and a ** (N-3) stage, it is also possible to lower power supply. Therefore, eye a ** (N-y) stage It is also possible to stop an electric power supply to a circuit of [y>=2], or to lower power supply.
[0046]In order to drive a liquid crystal, it is [5V grade] needed by potential difference from the transmissivity-voltage characteristic of a liquid crystal. However, since it deteriorates [having impressed direct current voltage to a liquid crystal and], it is necessary to make it an alternating current drive. About tenv of potential difference is needed, and power supply voltage of a circumference drive circuit is needed around 20 V.
[0047]Therefore, in a portion which does not specify a pixel among circumference drive circuits, power consumption is reducible by making power supply less than 20V. or a thing suspended for an electric power supply into a portion which does not specify a pixel -- the minimum -- it can be considered as required power consumption. Only when a circumference drive circuit is operated by less than 20V and it specifies a pixel, it can be said by considering it as power supply voltage of 20V that power consumption is reducible.
[0048]For example, when a thin film transistor and resistance constitute a counter circuit of a circumference drive circuit, a decoder circuit, etc., each circuit has large power consumption, but

power consumption can be stopped as a whole by operating only a portion which should function.

[0049]One of the composition of a liquid crystal electro-optic device built over this invention in order to cancel an above-mentioned problem. In a circumference drive circuit of a liquid crystal electro-optic device for driving a picture element part divided into two or more blocks so that two or more pixels might be arranged on a matrix and might contain said at least one pixel, Have a power supplying circuit which supplies electric power to this circumference drive circuit, and during said block, When a pixel in which voltage is impressed or a sampled BIO signal is written does not exist, Or when a pixel in which a sampled video signal is written does not exist, said power supplying circuit stops an electric power supply at least to a part corresponding to a pixel under said block among said circumference drive circuits. Or electric power supplies are reduced.
[0050]A circumference drive circuit which has the above-mentioned composition packs arbitrary numbers, considers a pixel as a block, and is controlling supply of electric power for every circuit corresponding to a pixel of the block. Therefore, a pixel is blocked, and a circumference drive circuit is also blocked and an electric power supply is controlled for every block. That is, he stops an electric power supply or is trying to lower power supply to a block which does not specify a pixel.
[0051]Numerals are attached for a circuit which specifies a pixel first one by one as the 1st block. When an input signal reaches the Nth block, an electric power supply to a block of ** (N-1) watch before is stopped, or power supply can be lowered. An electric power supply to a block of ** (N+1) watch henceforth is stopped, or power supply can be lowered.
[0052]An electric power supply to a block of eye ** (N+1) watch remains as it is, stops an electric power supply to a block of eye ** (N+2) watch, eye ** (N+3) watch, etc., or can lower power supply. Therefore, ** (N+x) stage It is also possible to stop an electric power supply to a block of [x>=1], or to lower power supply.
[0053]Or it supplies a power supply to a block of eye a ** (N-1) stage and does not supply electric power to a block of a ** (N-2) stage, a ** (N-3) stage, etc., it is also possible to lower power supply. Therefore, eye a ** (N-y) stage An electric power supply to a block of [y>=1] is stopped, or power supply can be lowered. It is also possible to drop power supply voltage of a circuit part.
[0054]
[Example]Drawing 3 is a partial circuit diagram of a shift register, and is illustrating only the register for three steps. Drawing 4 is a chart figure of the input output signal of three steps of registers.
[0055]In the following Examples 1-4, input and output of register ** take up the shift register used as what is shown in drawing 4 with composition as shown in drawing 3.
[0056][Example 1] In Example 1, a shift register is blocked and the case where an electric power supply is carried out for every block is shown. A CMOS circuit shall constitute the control circuit which controls an electric power supply out of the transparent substrate in which the picture element matrix was formed.
[0057]The case where eight steps of shift registers are 1 block is shown in drawing 5. Although it is also possible to detect an input signal and to make a control signal, it uses here that the control circuit (501) and the shift register (502) synchronize.
[0058]The signal from a clock oscillator (503) is inputted into a shift register (502) and the counter (504) of a control circuit (501). The output of a counter (504) serves as a control signal (506) by a decoder (505). A control signal (506) is inputted into a shift register (502).
[0059]drawing 6 -- the [of a shift register (502)] -- the timing chart of a control signal (506) to the block of eye N is shown. Based on the clock signal (601) of a clock oscillator (503), a decoder (502) creates a control signal (506). Three signals, an electric power supply signal (602), the clear signal (603) initialized at the time of the Nth shift register block starting, and clock supply signals (604), are created.
[0060]When eight steps of registers are 1 block, in addition to a thing period (605) required to make an output, it is begun for it to be begun at the time of (606) to supply electric power to a block, and to input a clock signal at the time of (607). The output at the time of starting is

ensured by establishing a time lag (608), without making simultaneous the input of an electric power supply and a clock signal.
[0061]After a signal is inputted into a ** (N+1) block from the Nth block, although the electric power supply to the Nth block may be stopped at any time, an electric power supply and clock supply are suspended here at the time of (609).
[0062]When eight steps of registers are 1 block, the circuit which makes the control signal (506) supplied to the 4th block is shown in drawing 7.
[0063]The output of the same clock oscillator (701) as the clock oscillator (503) of drawing 5 is inputted into a binary counter (702). The output of a binary counter (702) is detected by an AND circuit (703), (704), and (705), is compounded by an OR circuit (706) and (707), and is made into a control signal.
[0064]An AND circuit (703) selects during the period when an AND circuit (704) tells a clear period and an AND circuit (705) tells a clear period and an input signal for a period required in order that a shift register block may tell an input signal inside a block, respectively.
[0065]Therefore, about the output of an AND circuit (703), (704), and (705), if logical sum is taken by an OR circuit (706), it will become an electric power supply signal (602). What reversed the output of the AND circuit (704) with the inverter (708) serves as a clear signal (603), and an AND circuit (703) and the output of (705) serve as clock supply signals (604) by an OR circuit (708).
[0066]The circuit which supplies a power supply to a shift register block by P channel type TFT is shown in drawing 8.
[0067]A plus side power source line (801) is connected to a shift register block (803) through P channel type TFT (802).
[0068]An electric power supply signal (602) is impressed to the gate electrode of P channel type TFT (802).
[0069]A clear circuit is shown in drawing 9. P channel type TFT (902) which becomes final and conclusive the value of one step (901) of memory loop of a shift register at the time of starting is connected.
[0070]A clear signal (603) is impressed to the gate electrode of P channel type TFT (902).
[0071]In order to become final and conclusive the value of a loop so that the output of a buffer (903) may be before and after starting of a shift register and it may not change here, When the output of a buffer (903) is normal power supply potential, in the case of ground potential, the drain electrode of P channel type TFT (902) is usually connected to a point of contact (904) at a point of contact (905).
[0072]A clock supply circuit is shown in drawing 10. It lets P channel type TFT (1003) and (1004) pass, and a clock line (1001) and (1002) are connected to a shift register block (1005).
[0073]Clock supply signals (604) are impressed to P channel type TFT (1003) and the gate electrode of (1004).
[0074]About the shift register of this example, the power consumption at the time of using as a circumference drive circuit of a liquid crystal electro-optic device is measured. What broke the square of power supply voltage by resistance per resistance serves as power consumption in one resistance. In the case of the conventional example shown in drawing 32, a power supply is always supplied to those with three piece, and a whole page to 1 step of shift register middle resistance. Therefore, in the case of a conventional type, power consumption increases in proportion to the number of stages of a shift register.
[0075]However, in the case of Example 1, the resistance in one step of shift register is three pieces, but a power supply is always supplied to signal transduction by the lap of a control signal with eight steps of shift registers, and a contiguity block to the circuit of four steps of shift registers, and a power supply is not supplied to other shift registers. Therefore, even if power consumption as a circumference drive circuit can be made very small and the number of stages of a shift register increases, power consumption does not change.
[0076]If whether 640 steps of shift registers shall be operated and it specifically becomes a power-supply-potential output as the power supply voltage 20V and resistance 300komega or it becomes a ground potential output shall cut with the probability 1/2, In the composition of Example 1, the power consumption could be 24 mW to being 1280 mW with the conventional

type.
[0077][Example 2] In Example 2, a control circuit is provided for every register of a shift register, and the case where a special signal is used from the outside is shown.
[0078]As shown in drawing 11, a control circuit (1102) is provided for every register of a shift register (1101), an input signal (1103) is detected, and a control signal (1104) is created.
[0079]Since pulse width is not guaranteed if the electric power supply was carried out after the input signal reached, electric power is supplied before an input signal reaches. Electric power is supplied before the half cycle of a basic clock, a register is specifically started, and a basic clock suspends supply of electric power after 1 cycle (i.e., immediately after a register outputs actively).
[0080]The mimetic diagram explaining operation of a shift register is shown in drawing 12. Drawing 12 (a) shows the state where the Nth register is active, and drawing 12 (b) shows the state after clock 1 cycle from the state of drawing 12 (a). As shown in drawing 12 a, the output signal (1203) of the register (1202) of the Nth step of a shift register (1201) is inputted into the circuit (1205) of eye ** (N+1) watch of a control circuit (1204), and the circuit (1206) of eye ** (N-2) watch.
[0081]In the control circuit (1205) of eye ** (N+1) watch, if the output signal (1203) of the register (1202) of the Nth step becomes active, the control signal (1208) which supplies electric power to the register (1207) of eye the ** (N+1) stage will be created, and the register of eye the ** (N+1) stage will be started.
[0082]In the control circuit (1206) of eye ** (N-2) watch, if the output (1203) of the register (1202) of the Nth step becomes active, the control signal (1210) which stops an electric power supply to the shift register (1209) of eye the ** (N-2) stage will be created, and the register of eye the ** (N-2) stage will be suspended.
[0083]When the following clock pulse is inputted into a shift register (1201), as shown in drawing 12 (b), in the control circuit (1211) of eye ** (N+2) watch. If the output signal (1212) of the register (1207) of eye the ** (N+1) stage becomes active, the control signal (1214) which supplies electric power to the register (1213) of eye the ** (N+2) stage will be created, and the register of eye the ** (N+2) stage will be started.
[0084]In the control circuit (1215) of eye ** (N-1) watch. If the output (1212) of a ** (N+1) stage register (1207) becomes active, the control signal (1217) which stops an electric power supply to the shift register (1216) of eye the ** (N-1) stage will be created, and the register of eye the ** (N-1) stage will be suspended.
[0085]Whenever a clock signal is newly inputted into a shift register, the above operation is repeated, and a register is started and suspended one by one.
[0086]Even if it begins to supply electric power to a shift register, and it stops, as the sampler (105) of drawing 1 does not malfunction, the output of the buffer (104) of drawing 1 must not change. From now on, the output of the buffer (104) of drawing 1 is trustworthy, and the period which does not supply a power supply to the shift register (1101) of drawing 11 will consider the output of a buffer as the input of the register of the next step in Example 2 in consideration of the signal in a shift register (1101) being uncertain.
[0087]The timing chart for one step of register is shown in drawing 13 based on this. Nth-step adjustment input A (1303) power supply potential (1304) is made from the buffer output (1302) of a basic clock (1301) and the register of eye the ** (N-1) stage. Here, although one step of a register is operating by 1.5 cycles of a basic clock, since a control signal is late for the standup of a clock, and falling, as an input signal to the register of the Nth step, two cycles of a basic clock are made and pulse width is certainly considered as a part for basic clock 1 cycle.
[0088]That is, the power supply potential (1308) of the Nth-step adjustment input B (1307) is made from the buffer output (1306) of the inversion signal (1305) of a basic clock, and the register of eye the ** (N+1) stage. And logical sum is taken by making the input adjust signals A (1303) and B (1307) into an active high, and an adjust signal as shown in (1309) is made.
[0089]The way things stand, since the buffer output signal (1302) of the register of eye the ** (N-1) stage changes from a basic clock (1301) behind time, in (1310) of an adjust signal (1309), it produces a malfunction signal.
[0090]In this case, let operation be a positive thing by carrying out a mask with the clock (1311)

of the 1.5 time cycle of a basic clock. The buffer output (1312) of the register of the Nth step can be formed with these signals.
[0091]It seems that here shows the electric power supply signal in the Nth step to (1313). In order to avoid change of the input signal width by element delay, an electric power supply is begun before the half cycle of a basic clock when an input signal reaches.

[0092]What does not use a logic circuit as a control circuit since memory (maintenance of a state) is possible and low power consumption is called for is desirable. In Example 2, a frequency characteristic considers the circuit centering on a capacitor with easy composition of what worsening.
[0093]A control circuit is shown in drawing 14. A capacitor (1401) stops the electric power supply of a shift register, and makes the control signal output (1402) which supplies a power supply to a shift register by a discharge state from a charging state.
[0094]P channel type TFT (1403) sets up the initial state of a control circuit after powering on of the whole circuit. That is, before inputting an input signal into a shift register, a grand potential signal is impressed to the gate electrode of P channel type TFT (1403), and a capacitor (1401) is charged.
[0095]In the Nth control circuit, in order take an input signal and not to spill it, when an input signal reaches the register of eye the ** (N-1) stage, the register of the Nth step is started and an input signal is incorporated by the next clock change.
[0096]Therefore, P channel type TFT (1404) considers the buffer output of the register of eye the ** (N-1) stage as the input of a gate electrode. By this, if the buffer output of the register of eye the ** (N-1) stage becomes ground potential, a capacitor (1401) will be discharged and the signal which supplies a power supply to the register of the Nth step will be made.
[0097]Similarly, in the Nth control circuit, if an input signal reaches the register of eye the ** (N+2) stage, the register of the Nth step may be in the state where the active signal is not taken out, and may stop an electric power supply.
[0098]Therefore, P channel type TFT (1405) considers the buffer output of a ** (N+2) stage shift register as the input of a gate electrode. By this, if the buffer output of a ** (N+2) stage shift register becomes ground potential, a capacitor (1401) will be charged and the electric power supply of the shift register of the Nth step will be stopped. Here, (1406) is resistance for power supply protection.
[0099]The register and buffer of the Nth step are shown in drawing 15. About a signal conditioning part (1501), to the gate electrode of P channel type TFT (1502), a basic clock, The clock of the 1.5 time cycle for masks to the gate electrode of P channel type TFT (1503), The buffer output of the register of eye the ** (N-1) stage is impressed to the gate electrode of P channel type TFT (1504), and the signal (1303) in falling of the buffer output of TOREJISUTA of the Nth step, i.e., drawing 13, is made.
[0100]To the gate electrode of P channel type TFT (1505), reversal of a basic clock, The clock of the 1.5 time cycle for masks to the gate electrode of P channel type TFT (1506), The buffer output of a ** (N+1) stage shift register is impressed to the gate electrode of P channel type TFT (1507), and the standup of the buffer output of the register of the Nth step, i.e., the signal in drawing 13, (1307) is made.
[0101]Therefore, as an output of a signal conditioning part, it becomes a signal (1309) in drawing 13. Since P channel type TFT (1504) and (1507) are in an OFF state fundamentally and current does not usually flow into resistance (1508), a control signal is not inputted into a signal conditioning part.
[0102]Although the whole page was conventionally operated as a shift register, a control signal is impressed to the gate electrode of P channel type TFT (1590), (1510), and (1511), and low power consumption is planned with the whole shift register by stopping an unnecessary period and an electric power supply.
[0103]The output of a signal conditioning part (1501) is impressed to the gate electrode of P channel type TFT (1512) 1.5 times at the clock of a cycle, and the gate electrode of P channel type TFT (1513), and the buffer input of the period which does not constitute the memory loop is made.

[0104]The output of the inverter (1516) which constitutes the memory loop 1.5 times in the inversion signal of the clock of a cycle and the gate electrode of P channel type TFT (1515) is impressed to the gate electrode of P channel type TFT (1514).
[0105]Fundamentally, P channel type TFT (1515) and resistance (1517) constitute the inverter. The memory loop is made with this inverter and the inverter constituted from P CHINEYARU type TFT (1518) and resistance (1519).
[0106]P channel type TFT (1520) and resistance (1521) constitute a buffer. P channel type TFT (1522) is for preventing that become final and conclusive each output of a shift register, and it becomes impossible to secure the charging state of the capacitor of a control circuit here, when clearing.
[0107]If the current capacity of P channel type TFT is large, it is also possible to summarize P channel type TFT (1509) which supplies a power supply, (1510), and (1511) to one.
[0108]When pulse width of an input signal does not need to be guaranteed, it is circuitry of Example 2 and it is also possible to synchronize a control signal with a basic clock and to supply a power supply to one step of shift register by one cycle.
[0109]About the shift register of this example, the power consumption at the time of using as a circumference drive circuit of a liquid crystal electro-optic device is measured. What broke the square of power supply voltage by resistance per resistance serves as power consumption in one resistance. In the case of the conventional example shown in drawing 32, a power supply is always supplied for resistance to one step of register to those with three piece, and a whole page. Therefore, in the case of a conventional type, power consumption increases in proportion to the number of stages of a shift register.
[0110]However, in the case of the circumference drive circuit shown in Example 2, one step of register has three resistance, but a power supply is always supplied to three steps of registers, and electric power is not supplied to other registers. Therefore, even if power consumption as a circumference drive circuit can be made very small and the number of stages of a shift register increases, power consumption does not change.
[0111]If whether 640 steps of shift registers shall be operated and it specifically becomes a power-supply-potential output as the power supply voltage 20V and resistance 300komega or it becomes a ground potential output shall cut with the probability 1/2, In the composition of Example 2, the power consumption could be 6 mW to being 1280 mW with the conventional type.
[0112][Example 3] In a shift register, Example 3 shows the case where a control circuit is provided for every register. In Example 2, the circuit which carries out the mask of the clock for the portion which had prevented malfunction with the clock of the cycle 1.5 times is provided, and it corresponds. Therefore, the main leading about of a signal and a control circuit are the same as that of Example 2.
[0113]The timing chart of shift register 1 step is shown in drawing 16. In a signal conditioning part, the power supply potential (1604) of the Nth stage input (1603) is made from the buffer output (1602) of reversal (1601) of a basic clock, and the register of eye the ** (N-1) stage.
[0114]Although a clock (1605) is desirable in timing as a signal which makes the memory loop, since the control signal of the Nth step becomes as shown in (1606), the memory loop is formed immediately after starting (1607), and the Nth stage input (1603) is not received.
[0115]Then, the mask of the clock (1605) is carried out by a control signal (1606) and (1608), and a loop formation signal as shown in (1609) is made. The Nth-step buffer output (1610) is created by these.
[0116]The composition of the register of the Nth step is shown in drawing 17. About a signal conditioning part (1701), the buffer output of the register of eye the ** (N-1) stage is impressed to a basic clock and the gate electrode of P channel type TFT (1703), and signal setting out at the time of the Nth-step register starting is carried out to the gate electrode of P channel type TFT (1702).
[0117]The circuit (1704) which selects a clock to the gate electrode of P channel type TFT (1705) The Nth control signal, Reversal of a basic clock is impressed to the gate electrode (1706) of P channel type TFT at the control signal of eye ** (N+1) watch, and the gate electrode (1707) of P channel type TFT, and an output (1708) is obtained. The signal which forms the memory loop is made from taking reversal of a signal (1708).

[0118]The circuit (1709) and buffer circuit (1710) which constitute the memory loop are the same as Example 2. Here, electric power supply and P channel type TFT (1716) is a thing for clear execution P channel type TFT (1711), (1712), (1713), (1714), and (1715).
[0119]About the shift register of this example, the power consumption at the time of using as a circumference drive circuit of a liquid crystal electro-optic device is measured. what broke the square of power supply voltage by resistance per resistance -- 1 -- it becomes the power consumption of this resistance. As for resistance, in the case of the conventional example shown in drawing 34, a power supply is always supplied to one step of register to those with three piece, and a whole page. Therefore, in the case of a conventional type, power consumption increases in proportion to the number of stages of a register.
[0120]However, in the case of the circumference drive circuit shown in Example 3, one step of register has five resistance, but a power supply is always supplied to three steps of registers, and a power supply is not supplied to other shift registers. Therefore, even if power consumption as a circumference drive circuit can be made very small and the number of stages of a register increases, power consumption does not change.
[0121]If whether 640 steps of shift registers shall be operated and it specifically becomes a power-supply-potential output as the power supply voltage 20V and resistance 300komega or it becomes a ground potential output shall cut with the probability 1/2, In the composition of Example 3, the power consumption could be 10 mW to being 1280 mW with the conventional type.
[0122][Example 4] Example 4 shows the case where an electric power supply is considered as two cycles of a basic clock. Although 1.5 cycles of a basic clock were carrying out period supply of the power supply in Example 2 and Example 3, a circuit is simplified by considering it as two cycles in Example 4.
[0123]The flow of a signal is shown in drawing 18 a. The composition of a shift register (1801), a buffer (1802), and a control circuit (1803) does not change. If outputting of the register of the Nth step becomes carry out clock synchronization and active with the active output (1804) from TOREJISUTA of eye the **(N-1) stage, the output (1806) of the buffer (1805) corresponding to the register of the Nth step will be changed.
[0124]If it inputs into the control circuit (1807) of eye ** (N+2) watch, and the control circuit (1808) of eye ** (N-2) watch and the Nth-step buffer output becomes active, a buffer output (1806), An electric power supply signal (1809) is made in the control circuit (1807) of eye ** (N+2) watch, and a power supply stop signal (1810) is made in the control circuit (1808) of eye ** (N-2) watch.
[0125]The flow of the signal after a basic clock half cycle is shown in drawing 18 b from drawing 18 a. In Example 4, not the Nth buffer output but the output of the register of the Nth step is used as an input of the register of eye the ** (N+1) stage.
[0126]A time chart is shown in drawing 19. An input signal is incorporated with a clock (1901) and the memory loop consists of clock reversal (1902).
[0127]A control signal becomes as shown in (1903), and supplies a power supply by two cycles of a basic clock.
[0128]The output of the register of the Nth step becomes like the solid line of (1904). In the register of eye the ** (N+1) stage, since a signal is incorporated by a period (1905) and (1906), it does not need to become like the dotted line of (1904). As a signal inputted into the buffer to the register of the Nth step, when (1907) is used, malfunction sets by a buffer output (1908) and there is nothing.
[0129]A circuit diagram is shown in drawing 20. The output of the register (2001) of the Nth step turns into a buffer (2002) of the Nth step, and an input of the register of eye the ** (N+1) stage.
[0130]A buffer (2002) output turns into an input of the control circuit (2003) of ** (N+2) and eye watch (N-2), and makes a control signal.
[0131]A shift register connects to each inverter of the shift register of drawing 32 in series P channel type TFT (2004) which carries out an electric power supply, (2005), and (2006).
[0132]It is also possible to connect with a power supply via one P channel type TFT which packs into one point the source electrode of P channel type TFT (2007) which makes an inverter, (2008), and (2009), and controls an electric power supply.

[0133]A buffer circuit (2002) and a control circuit (2003) are the same composition as Example 2. That is, the input to the gate electrode of P channel type TFT (2011) which discharges the Nth control circuit capacitor (2010), It is a buffer output of eye ** (N-2) watch, and the input to the gate electrode of P channel type TFT (2012) which charges is a buffer output of eye ** (N+2) watch.
[0134]Here, P channel type TFT (2013) and (2014) are clock synchronization analog switches, and P channel type TFT (2015) and (2016) are the things for clear execution.
[0135]About the shift register of this example, the power consumption at the time of using as a circumference drive circuit of a liquid crystal electro-optic device is measured. What broke the square of power supply voltage by resistance per resistance serves as power consumption of one resistance. In the case of the conventional example shown in drawing 34, a power supply is always supplied for resistance to one step of shift register to those with three piece, and a whole page. Therefore, in the case of a conventional type, power consumption increases in proportion to the number of stages of a shift register.
[0136]However, in the case of the circumference drive circuit shown in Example 4, one step of shift register has three resistance, but a power supply is always supplied to four steps of shift registers, and a power supply is not supplied to other shift registers. Therefore, even if power consumption as a circumference drive circuit can be made very small and the number of stages of a shift register increases, power consumption does not change.
[0137]If whether 640 steps of shift registers shall be operated and it specifically becomes a power-supply-potential output as the power supply voltage 20V and resistance 300komega or it becomes a ground potential output shall cut with the probability 1/2, In the composition of Example 4, the power consumption could be 8 mW to being 1280 mW with the conventional type.
[0138]In the following Examples 5-7, when it specifies a pixel, the circuitry made into the value for which power supply voltage is needed is shown. This is also circuitry which drops again the power supply voltage of the portion which is not functioning.
[0139][Example 5] -- constituting a circumference drive circuit using a shift register circuit -- the one conductivity type TFT -- the case where a circuit is realized by P channel type TFT and resistance here is assumed. A shift register circuit is shown in drawing 21. As shown in drawing 21, by this example, three inverters (2102), (2103), (2104), two analog switches (2105), and the circuit that comprises (2106) are pointed out in one step (2101). Here, (2107) is a buffer which one [a buffer / an analog switch] and turns off an analog switch.
[0140]The power supply voltage in which a dotted line realizes low power consumption for the power supply voltage in which a solid line can drive a liquid crystal by drawing 22 is shown. Considering the voltage variability region of the video signal which makes a liquid crystal driven, about [20V] power supply voltage is required for the buffer which operates an analog switch. After this, the buffer output which, and is turned off usually serves as ground potential at the time of about [20V] power supply potential, and a sampling, as shown in (2201). [a buffer output] [the analog switch constituted from P channel type TFT] Therefore, the waveform (2202) which is usually ground potential and serves as about [20V] potential as a buffer input at the time of a sampling is needed.
[0141]Here, the shift register circuit which makes a buffer input is considered. It is thought that the shift register circuit is shifting the timing to sample as an input signal. Therefore, if power supply voltage to the register of the Nth step is made into about 20V when making the timing to sample in a shift register (i.e., when an input signal exists in the register of the Nth step), It is possible to make a liquid crystal drive through a buffer analog switch video signal. On the contrary, when an input signal does not exist, the power supply voltage of a shift register circuit can be dropped in the range in which a shift register circuit does not malfunction. In this circuitry, the power supply potential which makes a liquid crystal drive is not used constantly, but since it is possible to drop power supply voltage in the range which logic does not reverse, power consumption will be reduced.
[0142]The circuitry which supplies the power supply voltage which can drive a liquid crystal, and the power supply voltage which realizes low power consumption to one step (2301) of shift register circuit is shown in drawing 23. The power supply voltage (low voltage power) which makes power supply voltage (high voltage power) which can drive a liquid crystal by making P

channel type TFT (2302) into an ON state low power consumption by making P channel type TFT (2303) into an ON state is supplied.
[0143]The circuit which controls a power supplying circuit is shown in drawing 24. How to pull out a signal of operating the control circuit corresponding to the Nth step (2401) of a shift register circuit and a control circuit is shown in drawing 24.
[0144]The capacitor (2402) of the control circuit corresponding to the Nth step of a shift register circuit carries out the following operations. When the voltage which can drive a liquid crystal charges, the power supply voltage made into low power consumption is supplied to the Nth step of a shift register circuit. On the contrary, while the capacitor is discharging near the ground potential, the power supply voltage which can drive a liquid crystal is supplied to the Nth step of a shift register circuit.
[0145]Operation of a control circuit is as follows. First, P channel type TFT (2403) is beforehand made one, and a capacitor (2402) is charged at the potential which can drive a liquid crystal. P channel type TFT (2403) is turned OFF after charge. That is, in an initial state, the power supply potential made into low power consumption will be supplied. A buffer is connected to the gate electrode of P channel type TFT (2405) through the output of the register (2404) of eye the ** (N-1) stage.
[0146]By this, if an input signal arrives at the register circuit of eye the ** (N-1) stage, a capacitor will be discharged near the ground potential. The potential of a capacitor serves as a power-supply-voltage control signal which carries out clock synchronization and can drive a liquid crystal by P channel form TFT (2406). It becomes a power-supply-voltage control signal made into low power consumption via an inverter (2407).
[0147]Therefore, when the capacitor of the control circuit corresponding to the register of the Nth step discharges, the power supply voltage which can drive a liquid crystal is supplied to the register circuit of the Nth step, and the supply of a power supply made into low power consumption is suspended. When the power supply potential of a shift register becomes low, the control circuit where power supply potential is high is made to malfunction with the output of a shift register here. In order to avoid this, the buffer output constantly used with the power supply potential which can drive a liquid crystal was used.
[0148]Since a power source control signal may make an ON state simultaneously P channel type TFT (2302) and (2303) and a power supply may be short-circuited by the time lag of an inverter, By resistance (2408), the power-supply-voltage control signal which can drive a liquid crystal is made distorted, it delays that P channel type TFT (2302) will be in an ON state, and a power short circuit is avoided.
[0149]A buffer is connected to the gate electrode of P channel type TFT (2410) through the output of the register (2409) of eye the ** (N+1) stage. If an input signal reaches the register of eye the ** (N+1) stage, the power supply potential which can drive a liquid crystal will be charged for a capacitor. By this, the power supply voltage made into low power consumption is supplied to the register circuit of the Nth step, and supply of the power supply which can drive a liquid crystal is suspended.
[0150]In order to sample, only when making an analog switch one [this circuitry], power supply voltage can be set as a required value. In except said, the power consumption reduction in the whole circuit is realizable by considering it as the power supply voltage used as low power consumption.
[0151]Power consumption is measured about the circumference drive circuit of this example. What broke the square of power supply voltage by resistance per resistance serves as power consumption in one resistance. Suppose that the voltage 20V which can drive a liquid crystal is always impressed to the circuit shown in drawing 37. Whether per one step of register, resistance will be three pieces and resistance becomes 300komega and a ground potential output or it becomes a power-supply-potential output shall cut with one half of probability. Power consumption will be set to 1280 mW, if a shift register circuit is made into 640 stage constitution and a buffer is removed. On the other hand, in the case of this example, it is as follows. 5V, four resistance per one step of shift register, and resistance set to 300komega voltage which makes voltage which drives a liquid crystal 20V and low power consumption. The power supply voltage which can drive a liquid crystal will be supplied to two steps among 640

steps of shift register circuits, and the power supply voltage used as low power consumption will be supplied to 638 steps. From these assumption, power consumption is calculable with 111 mW.
[0152]Thus, power consumption is reducible by the circuitry by this example.
[0153][Example 6] In the following examples, a power supply is supplied only to the portion which specifies the pixel, and the circuitry which stops an electric power supply is shown in the portion which does not specify the pixel. In this example, the circumference drive circuit which specifies a pixel using a decoder circuit and a counter circuit is assumed.
[0154]The signal which specifies a pixel is made by letting the decoder circuit which constitutes the output (an inverted output is also included) of a counter circuit from a basic gate circuit shown by drawing 35 pass. Supposing it makes a decoder circuit use also [buffer], in order to reduce power consumption, the electric power of a counter circuit will be reduced. In the circuitry shown by drawing 37, since it is impossible, dividing a counter circuit into the portion which specifies a pixel, and the portion which is not specified divides a counter circuit.
[0155]One counter does not generate the address corresponding to a signal wire or a scanning line, but a counter circuit with little number of bits is used like drawing 25. Said counter circuit is pinpointed for a pixel by the required thing for which carry out part preparation, they are made to operate sequentially, and a local address is generated. By this, the electric power supply to the counter circuit which does not need to be operated can be stopped. Here, a decoder circuit and (2504) are control circuits the counter circuit which (2501) divided a picture element matrix and (2502), and (2503).
[0156]The counter circuit, decoder circuit, and control circuit which were divided into drawing 26 are shown. In the counter circuit (2601) of eye ** (N-1) watch, if a ripple carry arises, it is begun to supply a power supply to the Nth counter circuit (2602), and if the counter circuit (2603) of eye ** (N+1) watch begins to count, supply of the power supply of the Nth counter circuit will be suspended.
[0157]the one conductivity type TFT that the control circuit is the same as Example 5, and for initial setting -- here -- a P channel type, [TFT and (2604)] In order to stop P channel type TFT (2605) and the electric power supply which discharge a capacitor in order to begin an electric power supply, it comprises a capacitor (2607) for P channel type TFT (2606) which charges a capacitor, and hold stores. When the Nth counter circuit begins to supply a power supply, the output value is unfixed. Therefore, a clearance is performed, when the ripple carry of the counter circuit of eye ** (N-1) watch arises and it begins to supply a power supply. The circuit which generates a clear signal comprises P channel type TFT (2608).
[0158]The circuit which supplies a power supply is realizable by connecting P channel type TFT in series, and controlling an electric power supply by this P channel type TFT between the source electrode of P channel type TFT of drawing 22, and a power supply. In drawing 26, P channel type TFT which makes additional connection in series is put together, and P channel type TFT (2609) shows. The enable signal to the Nth counter circuit (2602) is supplied by P channel form TFT (2609).
[0159]The output of the decoder circuit (2610) which detects the minimum output of the counter circuit of eye ** (N+1) watch is used for the power supply stop of the Nth counter circuit.
[0160]The timing chart of the Nth counter circuit is shown in drawing 27. The clear signal (2703) of the Nth counter circuit is formed immediately after a power supply (2701) injection by the ripple carry (2702) of the counter circuit of eye ** (N-1) watch. The output (2704) of the Nth counter circuit is inputted into a decoder circuit, and a decoded signal (2705) is made. By the following clock pulse which outputted the ripple carry, the electric power supply to the Nth counter circuit is stopped.
[0161]Power consumption is measured about the circumference drive circuit of this example. What broke the square of power supply voltage by resistance per resistance serves as power consumption in one resistance. Supposing it generates an address signal to 640 pixels, a 10-bit counter is needed. 1 bit of counters are equivalent to one JK-flip-flop, and since they are 10 gate necessity, one JK-flip-flop has the resistance which will connect a ground with a power supply only by 100 JK flip-flops. 16 gates are needed for others and there is one resistance which will connect a ground with a power supply per gate. Therefore, the resistance which will connect a ground with a power supply will be a total of 116 pieces. Resistance is set to

300komega and power supply voltage is set to 20V. Whether it becomes a ground potential output or it becomes a power-supply-potential output shall cut with one half of probability. Power consumption will be set to 77 mW if the decoder circuit of buffer combination is removed.
[0162]On the other hand, in the case of this example, it is as follows. Since four bit counters are used one by one regardless of a pixel number, it can be considered that four bit counters are usually operating. That is, the resistance of JK-flip-flop is ten pieces per four pieces and JK-flip-flop. Since the number of gates required between JK-flip-flops is eight, the resistance which will connect a ground with a power supply will be a total of 48 pieces. Resistance is set to 300komega and power supply voltage is set to 20V. Whether it becomes a ground potential output or it becomes a power-supply-potential output shall cut with one half of probability. Power consumption will be set to 32 mW from this assumption, if the decoder circuit of buffer combination is removed.
[0163]In the circumference drive circuit composition of only a decoder circuit and a counter circuit, power consumption increases in logarithm with the increase in a scanning line or a signal wire, but when it is this example, the increase in power consumption is not generated in circuit. Thus, it turns out by the circuitry by this example that power consumption is reducible.
[0164][Example 7] In the following examples, when it specifies a pixel, the circuitry made into the value for which power supply voltage is needed is shown. This is also circuitry which drops again the power supply voltage of the portion which is not functioning.
[0165]This example assumes the circumference drive circuit which specifies a pixel using a decoder circuit and a counter circuit like Example 6. However, let a counter circuit be 6 bit outputs.
[0166]Circuitry is shown in drawing 28. A control circuit (2801) is the same composition as Example 5. The signal which starts an electric power supply uses the ripple carry of the counter circuit (2803) of eye ** (N-1) watch for the Nth counter circuit (2802). The output of the decoder circuit (2805) which detects the minimum output of the counter circuit (2804) of eye ** (N+1) watch is used for the signal which stops an electric power supply to the Nth counter circuit. As an enable signal of the Nth counter circuit, the signal which controls the power supply voltage made into low power consumption is used. From now on, the Nth counter circuit will wait for an enable signal to become active next by a cleared condition. Therefore, even if power supply voltage changes, it is not necessary to perform a clearance.
[0167]Power consumption is measured about the circumference drive circuit of this example. What broke the square of power supply voltage by resistance per resistance serves as power consumption in one resistance. Supposing it generates an address signal to 640 pixels, a 10-bit counter is needed. 1 bit of counters are equivalent to one JK-flip-flop, and since they are 10 gate necessity, the resistance by which a ground is connected with a power supply has them in one JK-flip-flop only by 100 JK flip-flops. 16 gates are needed for others and there is one resistance which will connect a ground with a power supply per gate. Therefore, the resistance by which a power supply and a ground are touched will be a total of 116 pieces. Resistance is set to 300komega and power supply voltage is set to 20V. Whether it becomes a ground potential output or it becomes a power-supply-potential output shall cut with one half of probability. Power consumption will be set to 77 mW if the decoder circuit of buffer combination is removed.
[0168]On the other hand, in the case of this example, it is as follows. Six bit counters [11] are required to 640 pixels. Among these, the voltage 5V which makes voltage 20V which can drive a liquid crystal to one piece low power consumption to remaining ten pieces is supplied. In 6 bit counter circuits, the resistance of JK-flip-flop is ten pieces per six pieces and JK-flip-flop. Since the number of gates required between JK-flip-flops is 12, the resistance which will connect a ground with a power supply will be a total of 72 pieces. Resistance shall be set to 300komega and whether it becomes a ground potential output or it becomes a power-supply-potential output shall cut with one half of probability. Power consumption will be set to 62 mW from this assumption, if the decoder circuit of buffer combination is removed. By the circuitry by this example, power consumption is reducible.
[0169]
[Effect of the Invention]In a circumference drive circuit, since this invention supplies electric

power to the circuit which should operate, and stops an electric power supply in the other circuit or power supply was lowered, it can reduce the power consumption of the whole circuit. Malfunction of the circuit which should not operate can be prevented.
[0170]Even when the big circumference drive circuit of the power consumption especially constituted by a thin film transistor and resistance was used, it was able to be considered as power consumption very low as the whole circumference drive circuit. For example, since that operating power is supplied is only a register into which the signal is inputted even if the number of stages of a shift register increases, power consumption does not increase.
[0171]

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is an outline lineblock diagram of the liquid crystal electro-optic device for explaining an operation of this invention.
[Drawing 2]It is a block circuit diagram of the shift register for explaining an operation of this invention.
[Drawing 3]It is a lineblock diagram of the shift register of Examples 1-4.
[Drawing 4]It is a timing chart figure of the input output signal of the shift register of Examples 1-4.
[Drawing 5]It is a block circuit diagram of the shift register of Example 1.
[Drawing 6]The timing chart of a shift register is shown.
[Drawing 7]It is a lineblock diagram of a decoder circuit.
[Drawing 8]It is a lineblock diagram of a power supplying circuit.
[Drawing 9]It is a lineblock diagram of a clear circuit.
[Drawing 10]It is a lineblock diagram of a clock supply circuit.
[Drawing 11]It is a block circuit diagram of the shift register of Example 2.
[Drawing 12]It is a mimetic diagram showing operation of a shift register.
[Drawing 13]It is a timing chart figure of one step of register.
[Drawing 14]It is a lineblock diagram of a control circuit.
[Drawing 15]They are one step of shift register, and a lineblock diagram of one step of buffer.
[Drawing 16]It is a timing chart figure of one step of register of Example 3.
[Drawing 17]They are a register, a clock selection circuit, and a lineblock diagram of one step of buffer.
[Drawing 18]It is a lineblock diagram of a block showing operation of the shift register of Example 4.
[Drawing 19]It is a timing chart figure of 1 step of register **.
[Drawing 20]They are one step of shift register, a control circuit, and a lineblock diagram of one step of buffer.
[Drawing 21]It is a lineblock diagram of the shift register by the one conductivity type TFT of Example 5.
[Drawing 22]It is a timing chart figure of a shift register.

[Drawing 23]It is a lineblock diagram of the power-supply-voltage switching circuit by the one conductivity type TFT.
[Drawing 24]It is a lineblock diagram of other power-supply-voltage switching control circuits.
[Drawing 25]It is the counter and the lineblock diagram of a decoder which Example 6 divided.
[Drawing 26]They are a power supply stop type counter of Example 6, and a lineblock diagram of a control circuit.
[Drawing 27]It is a lineblock diagram of the timing chart of the counter circuit of Example 6.
[Drawing 28]They are a source-voltage-lowering type counter of Example 7, and a lineblock diagram of a control circuit.
[Drawing 29]It is a lineblock diagram of the circumference drive circuit of the liquid crystal electro-optic device of the conventional example 1.
[Drawing 30]It is a lineblock diagram of the shift register constituted with the clocked inverter, and the shift register constituted by the transmission gate.
[Drawing 31]It is a lineblock diagram of a signal line driving circuit using an address decoder.
[Drawing 32]They are a counter and a lineblock diagram of a signal line driving circuit using an address decoder.
[Drawing 33]It is a lineblock diagram of the shift register of the clocked inverter composition of a CMOS circuit.
[Drawing 34]It is a lineblock diagram of the shift register constituted from P channel type TFT and resistance.
[Drawing 35]It is a lineblock diagram of the basic gate circuit by the one conductivity type TFT.
[Drawing 36]It is a lineblock diagram of JK-flip-flop.
[Drawing 37]It is a lineblock diagram of four bit counters.
[Description of Notations]
101 ... Display matrix part
102, 108 ... Shift register
103, 106, 107, 110-112 ... Shift register block
104, 109 ... Buffer
105 ... Sampling circuit
401 Shift register
402-404 ... Shift register block
405 ... Control circuit
406, 407 ... Power supply stop signal
408 ... Electric power supply signal
409 ... Input signal which should be transmitted

[Translation done.]

* NOTICES *

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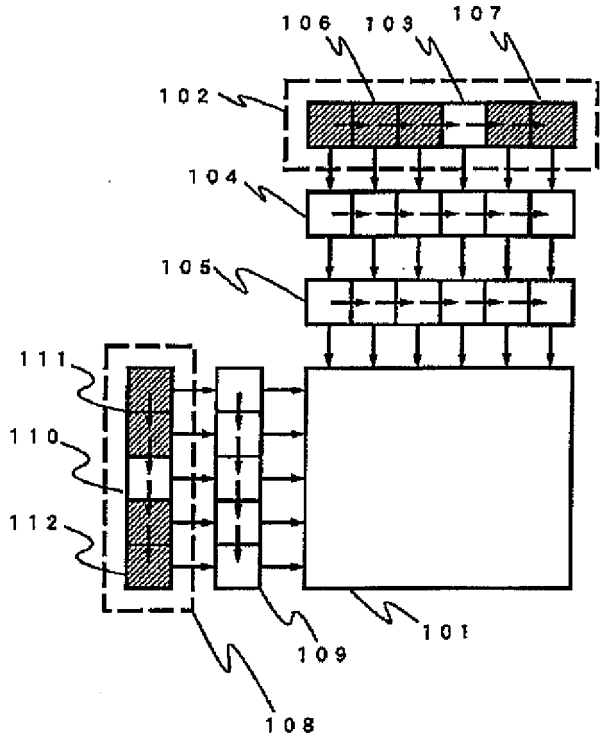
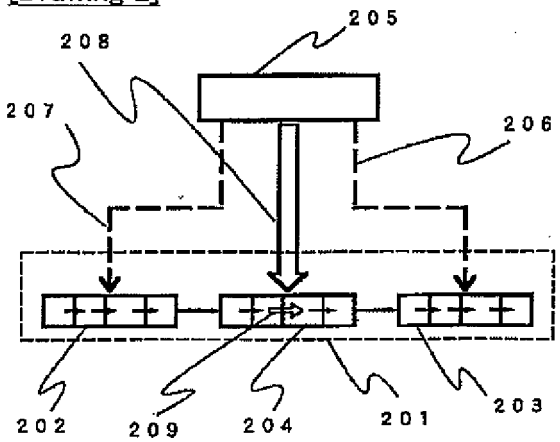
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

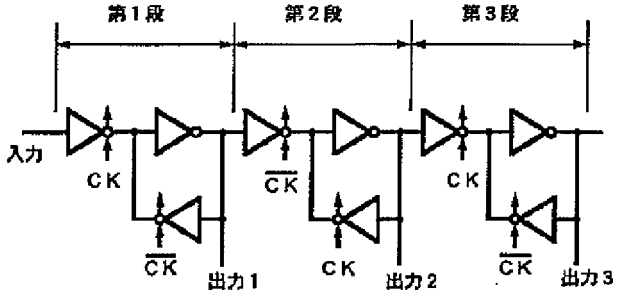
[Drawing 1]



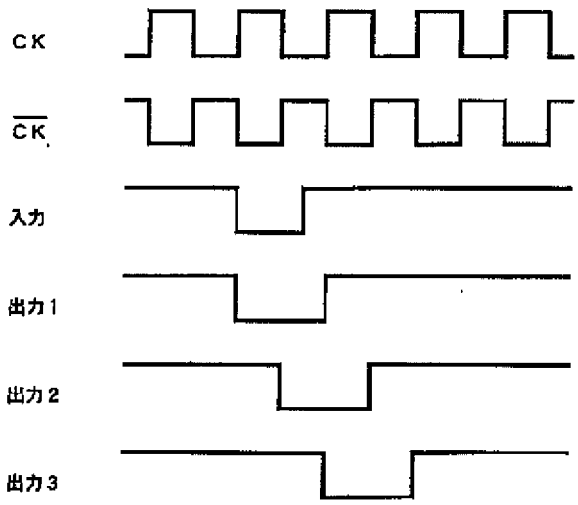
[Drawing 2]



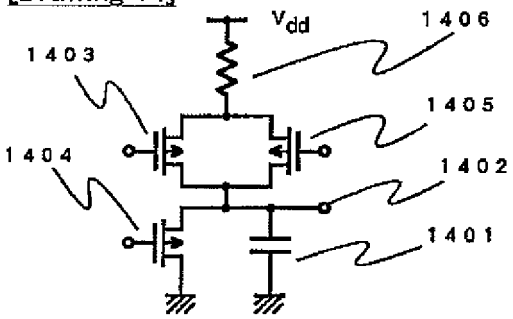
[Drawing 3]



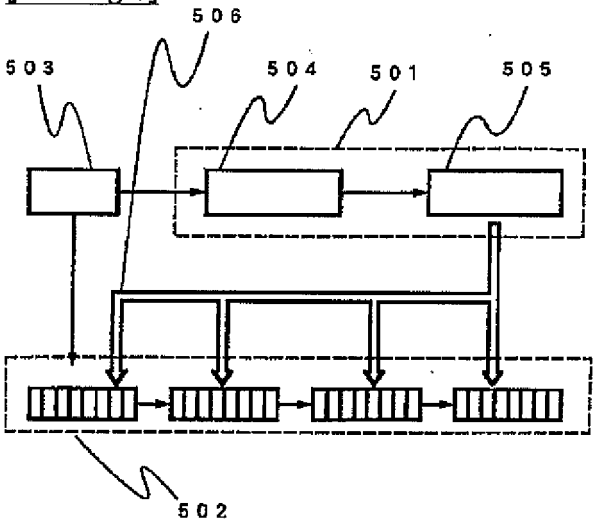
[Drawing 4]



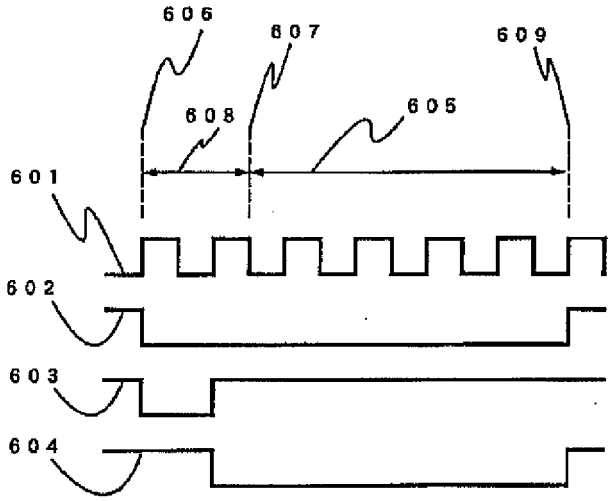
[Drawing 14]



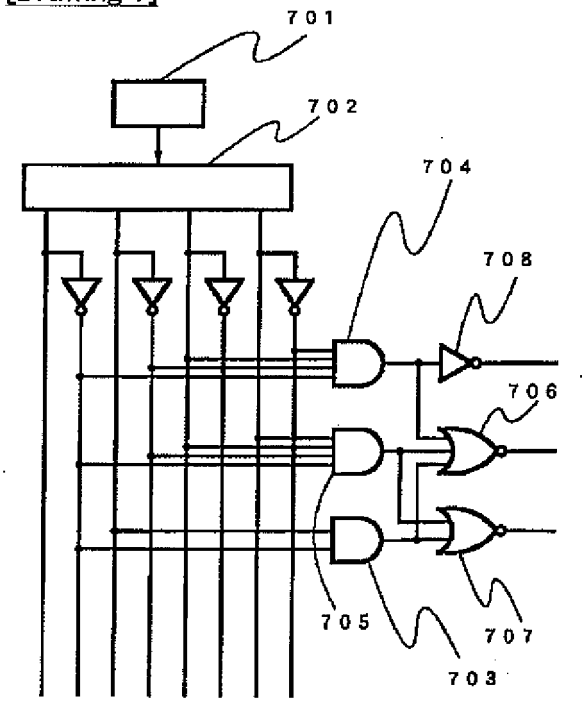
[Drawing 5]



[Drawing 6]



[Drawing 7]



[Drawing 8]

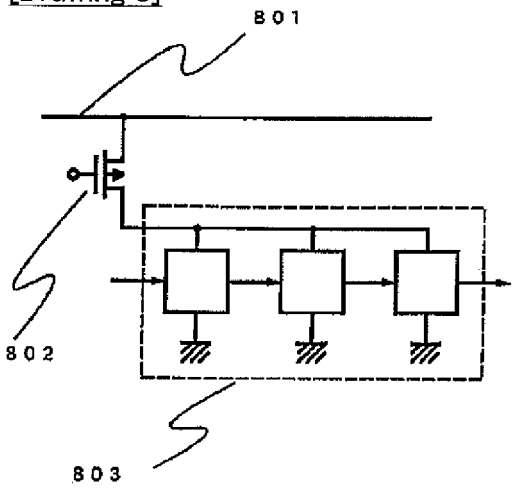
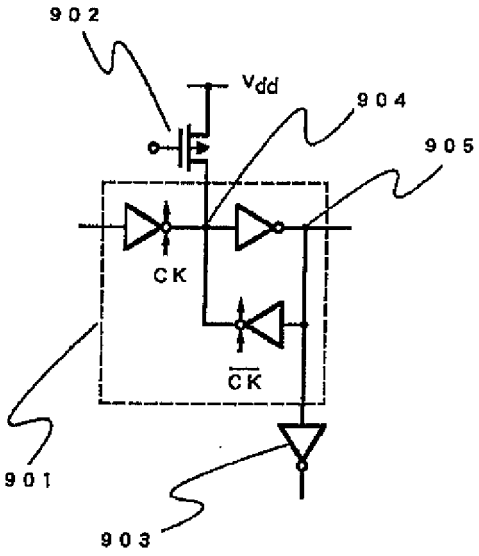
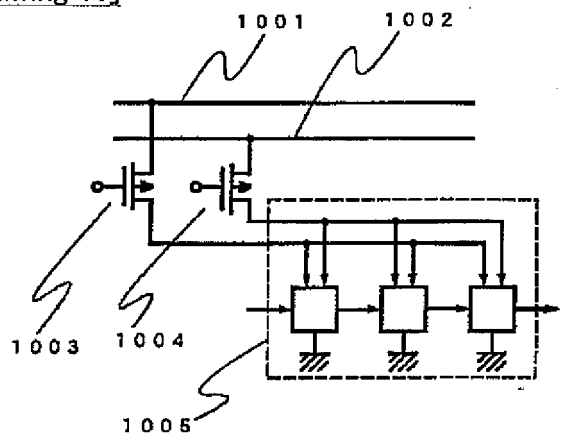


FIG. 8

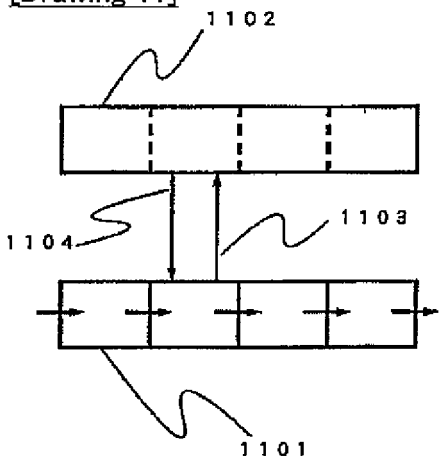
[Drawing 9]



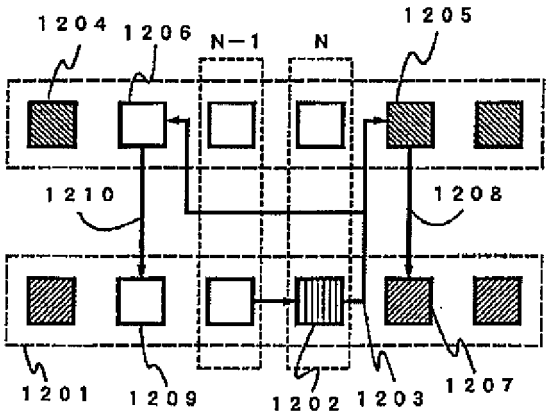
[Drawing 10]



[Drawing 11]



[Drawing 12]



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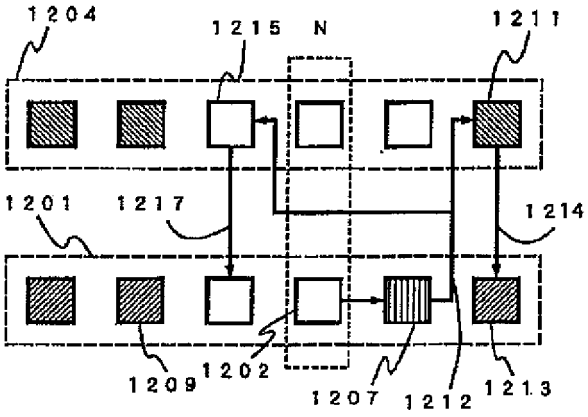
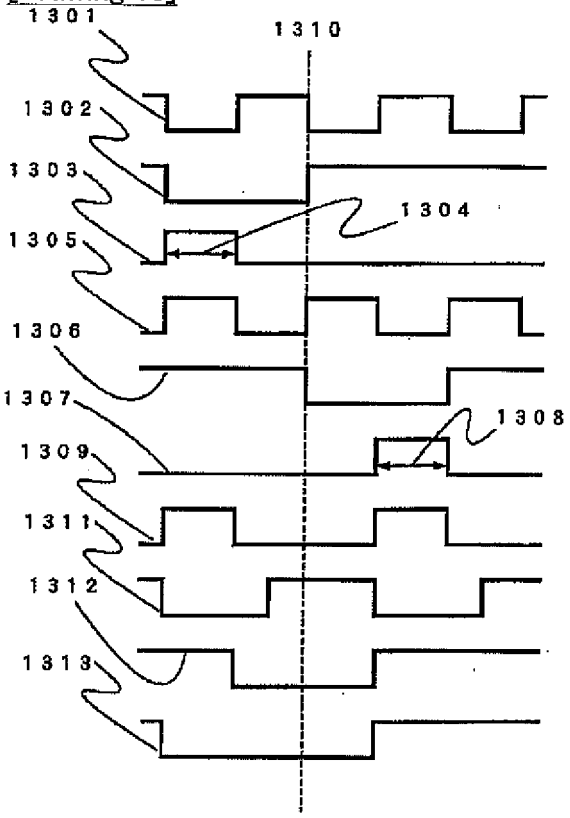
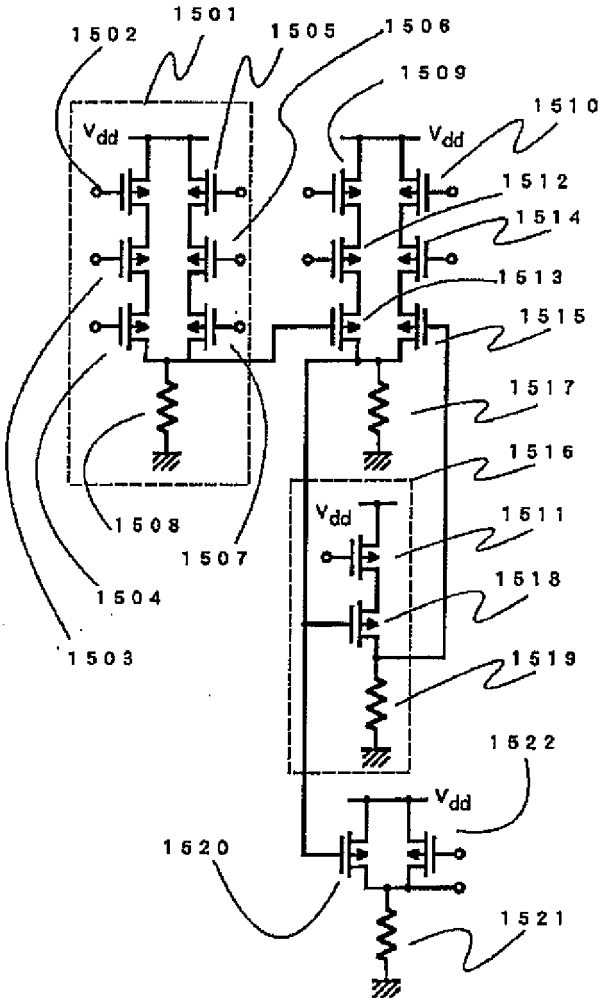


(b)

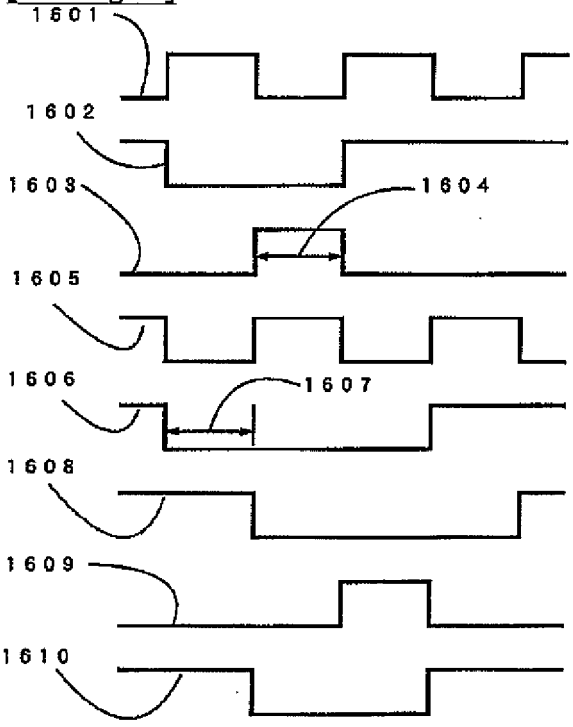
[Drawing 13]



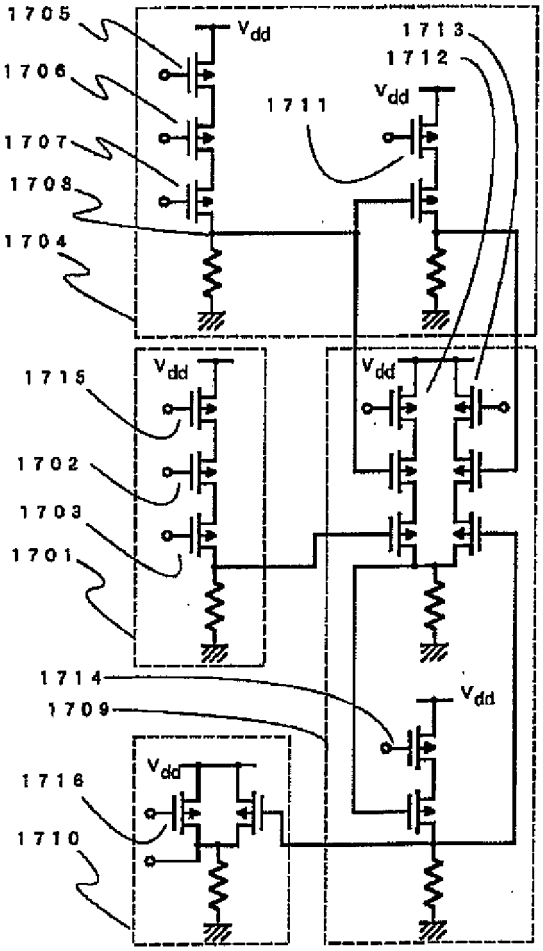
[Drawing 15]



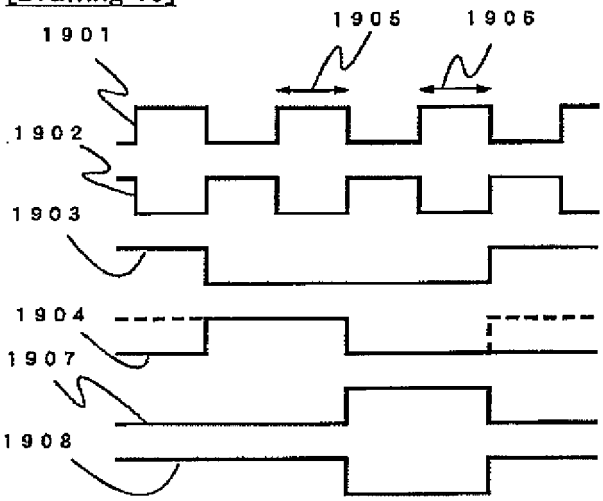
[Drawing 16]



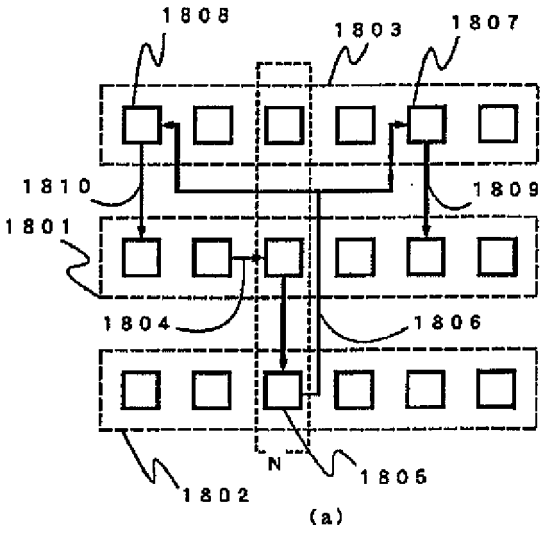
[Drawing 17]



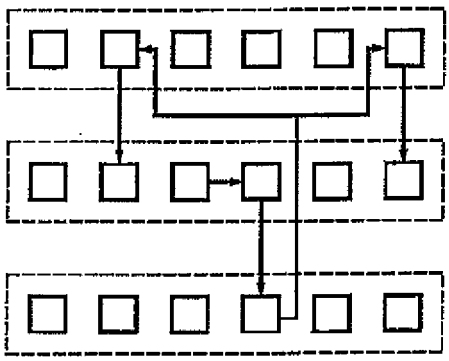
[Drawing 19]



[Drawing 18]

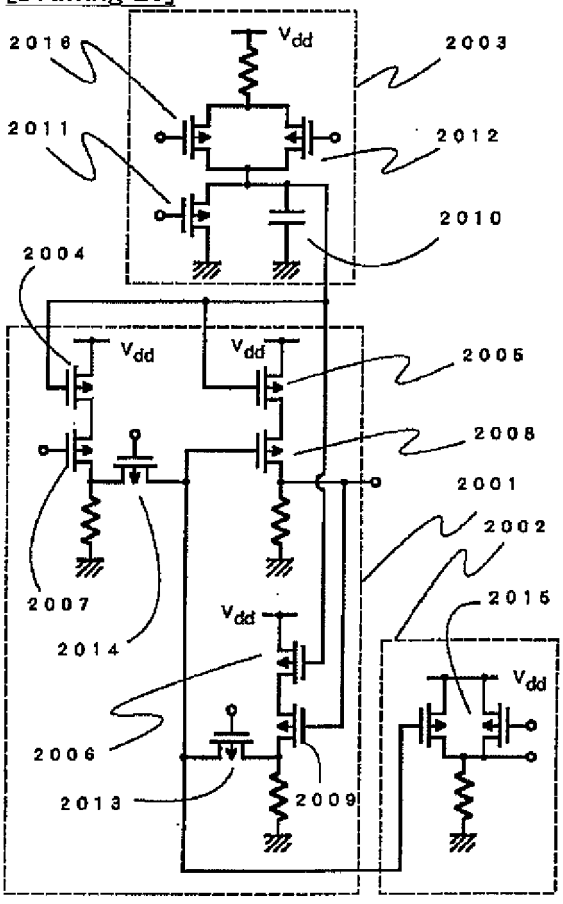


(a)

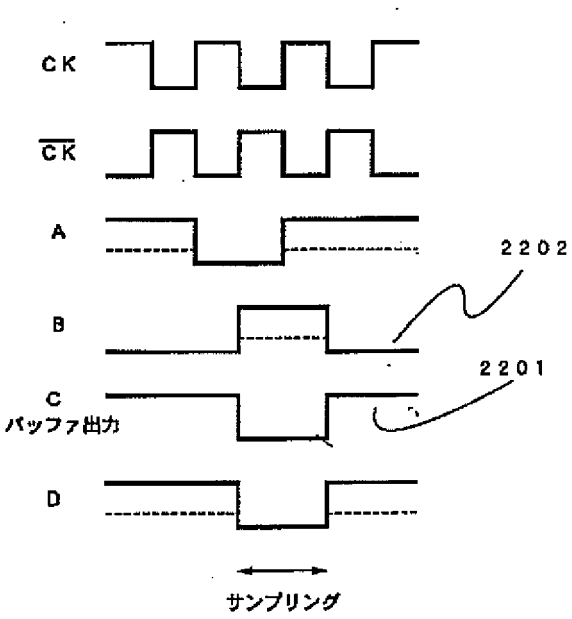


(b)

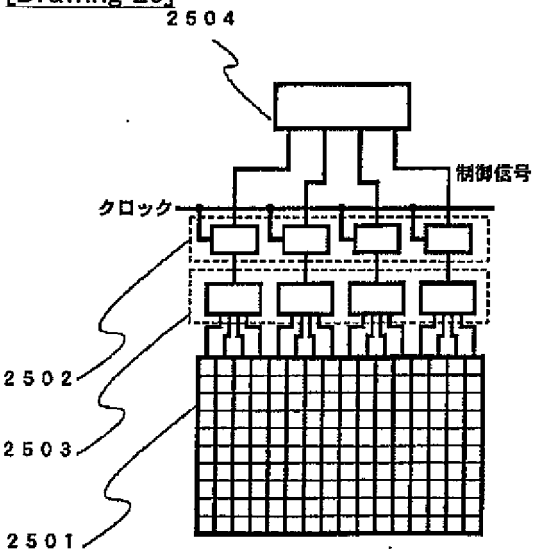
[Drawing 20]



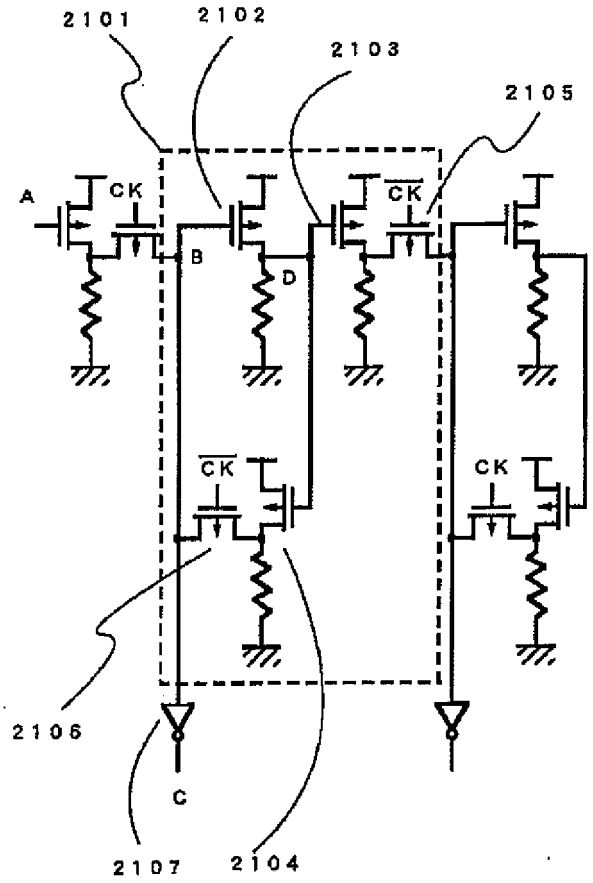
[Drawing 22]



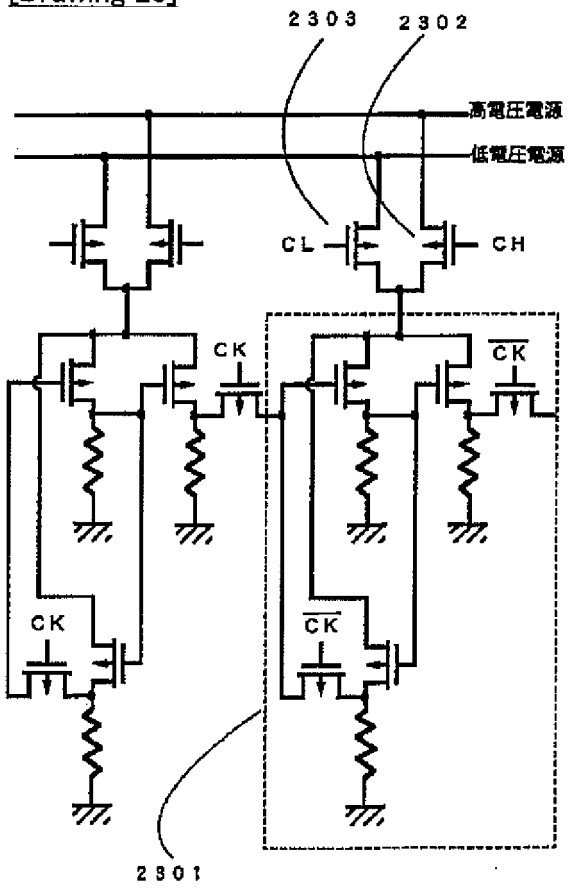
[Drawing 25]



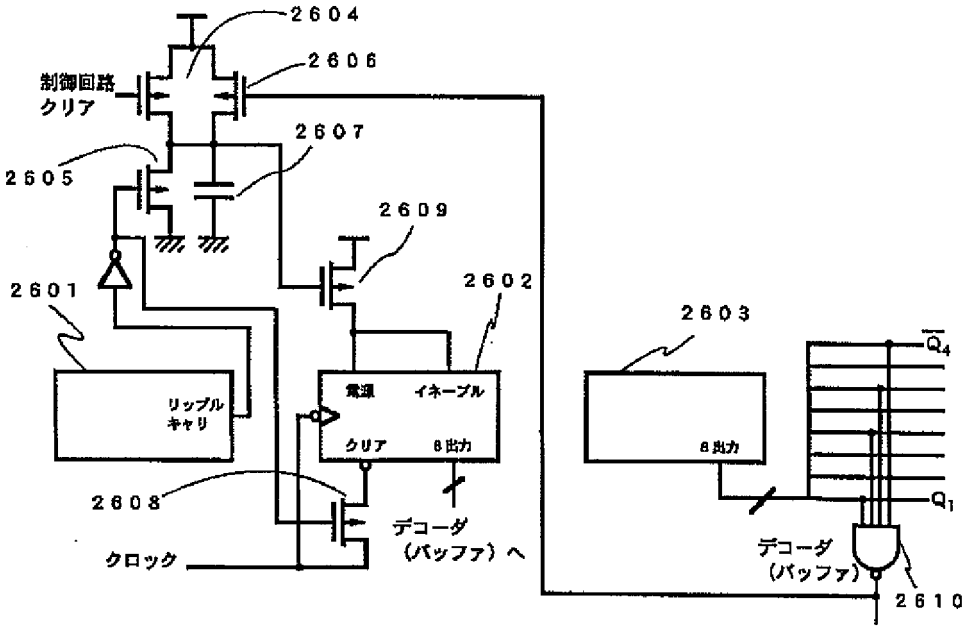
[Drawing 21]



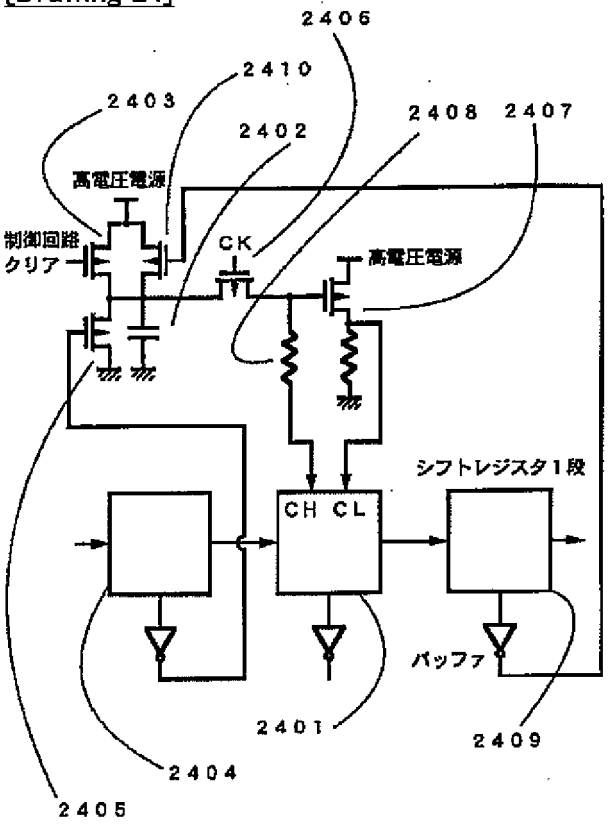
[Drawing 23]



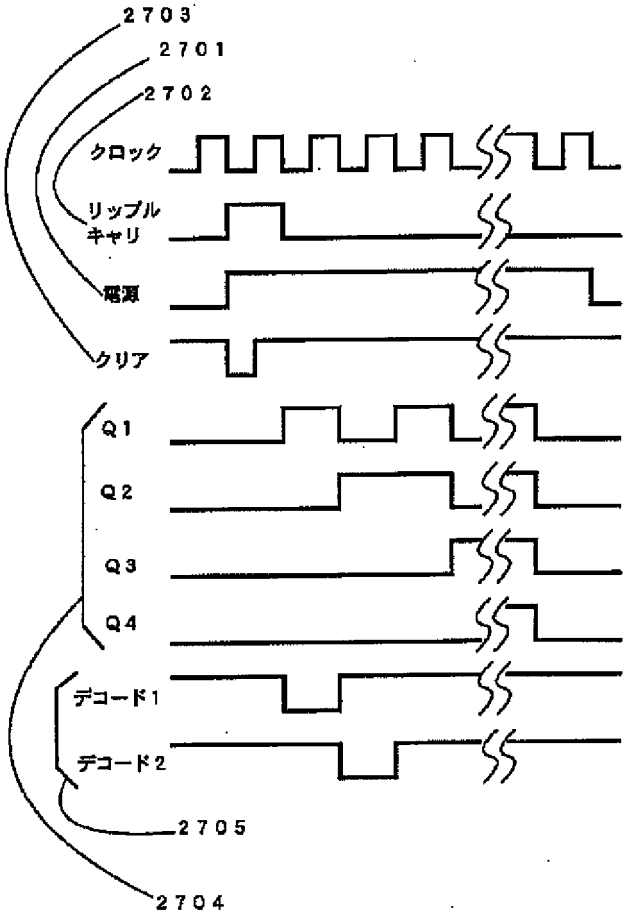
[Drawing 26]



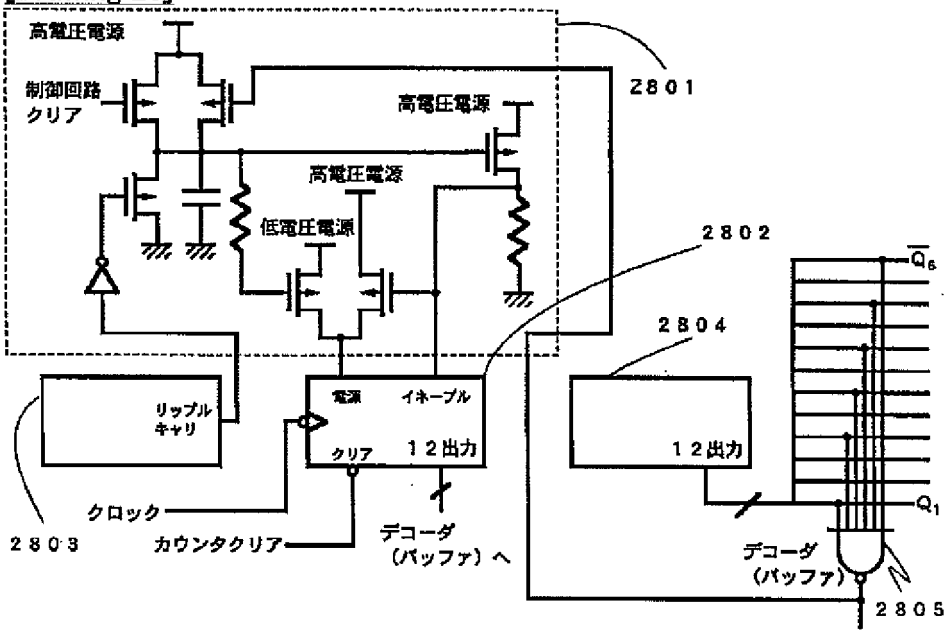
[Drawing 24]



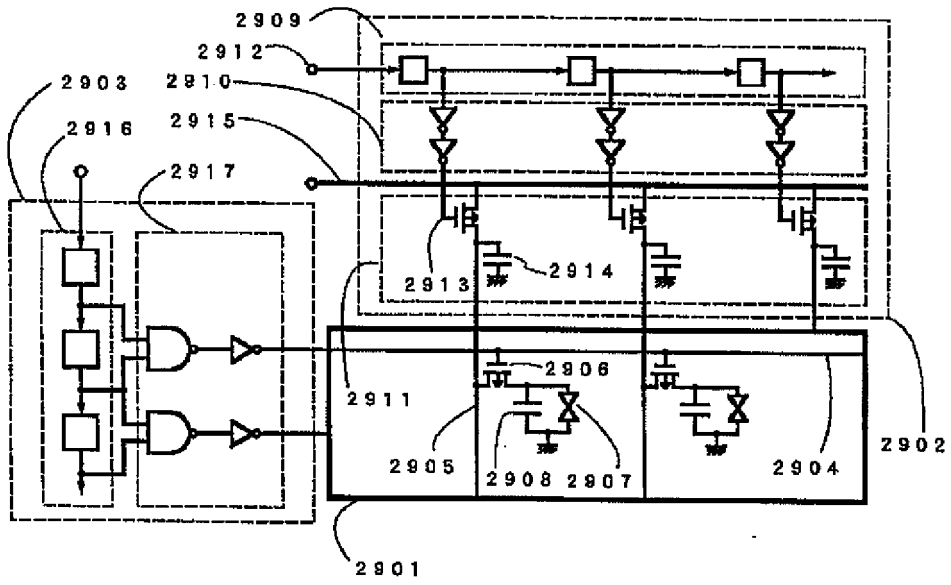
[Drawing 27]



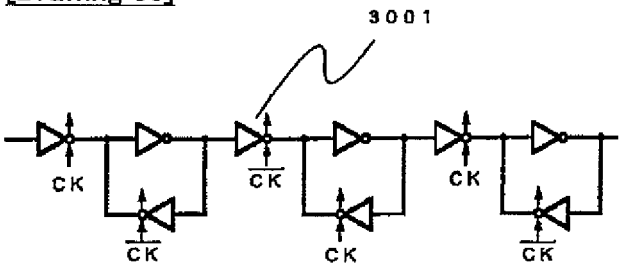
[Drawing 28]



[Drawing 29]



[Drawing 30]



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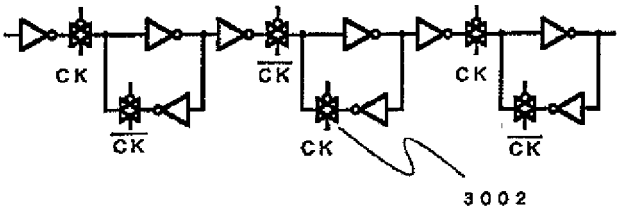
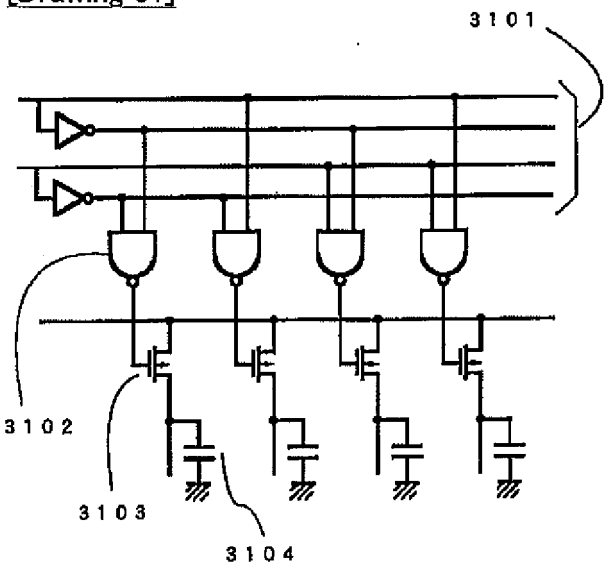
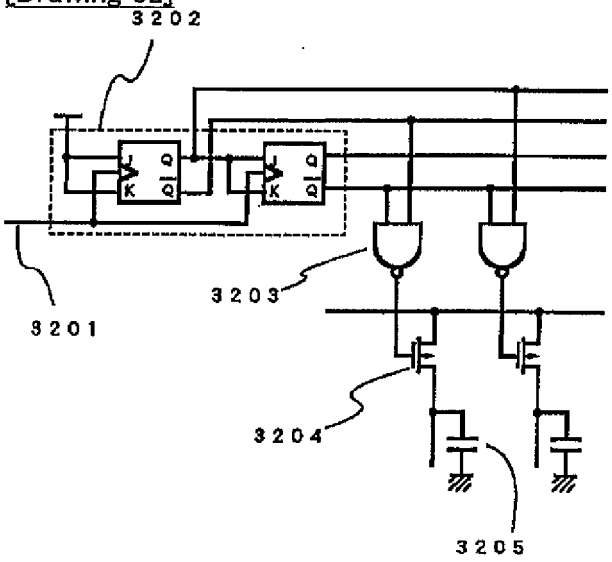


(b)

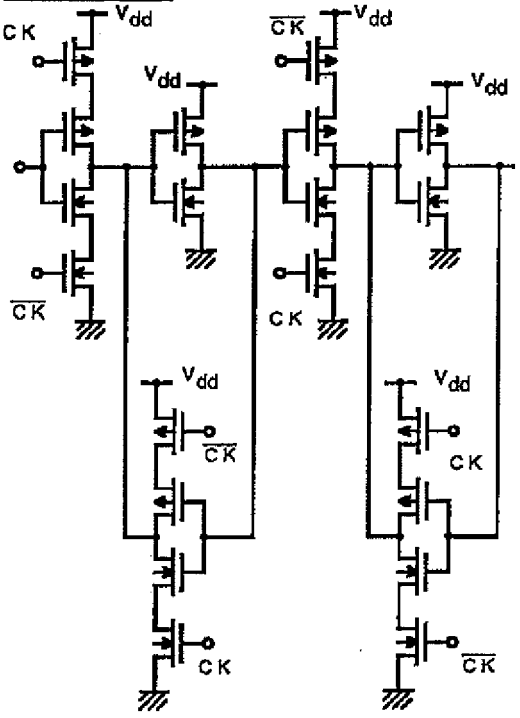
[Drawing 31]



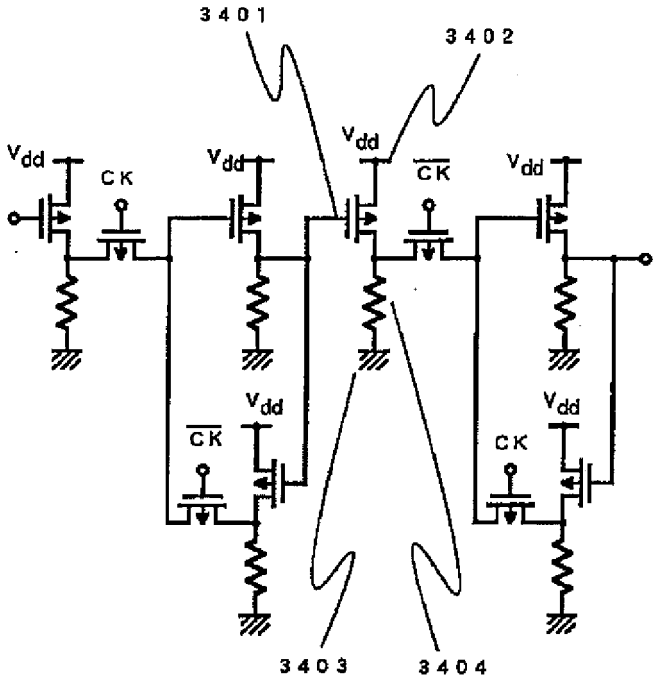
[Drawing 32]



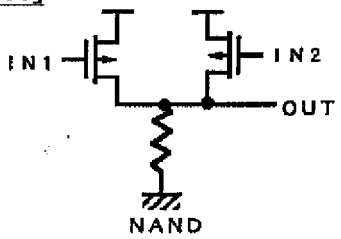
[Drawing 33]

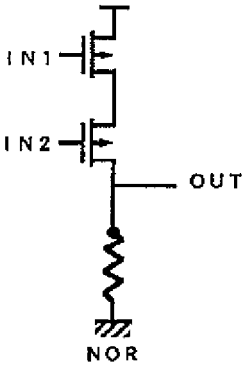


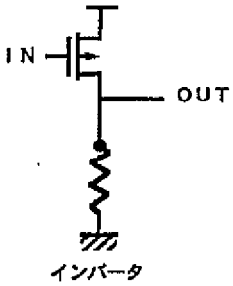
[Drawing 34]



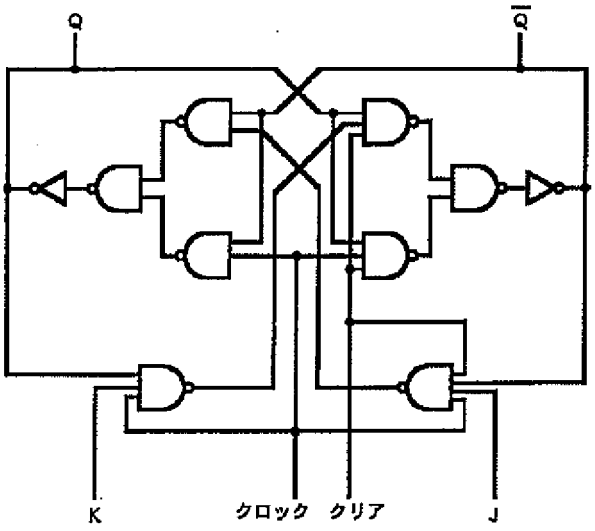
[Drawing 35]



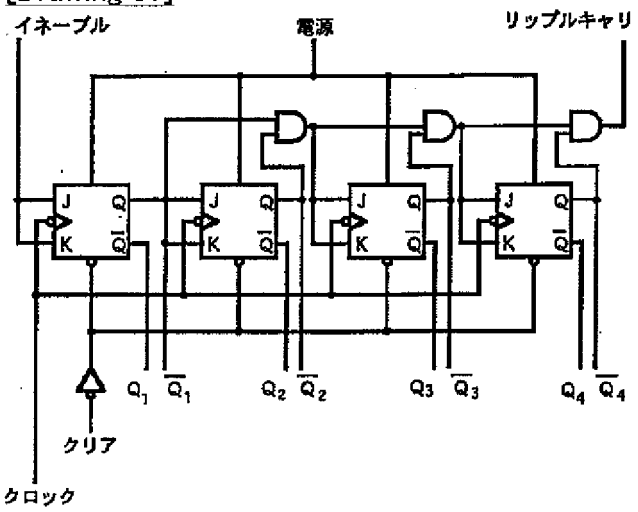




[Drawing 36]



[Drawing 37]



[Translation done.]